CMOS Logic Gates

The Inverter

Assume $V_{T0} < V^+$ for $M_1$ and $M_2$

$V_I = V^+ \Rightarrow V_{GS1} = V^+ > V_{T0}$
$V_{GS2} = 0 < V_{T0}$
$\Rightarrow M_1$ is ON
$M_2$ is OFF
$\Rightarrow V_O = 0$

$V_I = 0 \Rightarrow V_{GS2} = V^+ > V_{T0}$
$V_{GS1} = 0$
$\Rightarrow M_1$ is OFF
$M_2$ is ON
Let \( L = 0 \) \( H = V^+ \). The gate performs the following operations:

\[
\begin{align*}
V_I &= L & V_O &= H \\
V_I &= H & V_O &= L
\end{align*}
\]

We can plot \( V_O \) versus \( V_I \) as follows:

The noise margin is defined in terms of the voltages \( V_{IL} \), \( V_{IH} \), \( V_{OL} \), and \( V_{OH} \). The noise margins are figures of merit which relate to the susceptibility of the gate being switched by undesirable
noise at its input. To see how they are defined, consider the following circuit:

![Circuit Diagram]

Let \( V_{0A} \) be connected to \( V_{IA} \). If \( V_{0A} = L \), \( V_{0B} = H \) if \( V_{OLA} < V_{ILB} \). We define the low noise margin as

\[ NML = V_{ILB} - V_{OLA} \]

For identical gates, this becomes

\[ NML = V_{IL} - V_{OL} \]

If \( V_{0A} = H \), \( V_{0B} = L \) if \( V_{OLA} < V_{IHB} \). We define the high noise margin
as

\[ \text{NM}_{\text{H}} = \text{V}_{\text{OH}} - \text{V}_{\text{IH}} \]

For identical gates, this becomes

\[ \text{NM}_{\text{H}} = \text{V}_{\text{OH}} - \text{V}_{\text{IH}} \]

The larger \( \text{NM}_{\text{L}} \) and \( \text{NM}_{\text{H}} \), the more immune the gates are to false triggering by unavoidable noise voltages at its input.

If the two MOSFETs have the same value for \( V_{\text{TO}} \), it can be shown that

\[ V_{\text{IL}} = \frac{3V^+ + 2V_{\text{TO}}}{8} \quad V_{\text{IH}} = \frac{5V^+ - 2V_{\text{TO}}}{8} \]

\[ V_{\text{OL}} = \frac{V^+ - 2V_{\text{TO}}}{8} \quad V_{\text{OH}} = \frac{7V^+ + 2V_{\text{TO}}}{8} \]
These equations give

\[ N_{M_L} = N_{M_H} = \frac{V^+ + 2V_{TO}}{4} \]

In practice, \( V_{TO} \leq \frac{1}{2} V^+ \). For \( V_{TO} = \frac{1}{2} V^+ \), we have

\[ N_{M_L} = N_{M_H} = \frac{1}{2} V^+ \]

The CMOS NOR Gate

\[ A \quad B \quad Z \]
\[ \begin{array}{ccc}
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 0 \\
\end{array} \]

\[ Z = \overline{A \cdot B} \]
\[ V_A = L \quad V_B = L \]
\[ \Rightarrow M_1 \text{ off, } M_2 \text{ off, } M_3 \text{ on, and } M_4 \text{ on} \]
\[ \Rightarrow V_o = H \]

\[ V_A = L \quad V_B = H \]
\[ \Rightarrow M_1 \text{ off, } M_2 \text{ on, } M_3 \text{ off, and } M_4 \text{ on} \]
\[ \Rightarrow V_o = L \]

\[ V_A = H \quad V_B = L \]
\[ \Rightarrow M_1 \text{ on, } M_2 \text{ off, } M_3 \text{ off, and } M_4 \text{ off} \]
\[ \Rightarrow V_o = L \]

\[ V_A = H \quad V_B = H \]
\[ \Rightarrow M_1 \text{ on, } M_2 \text{ on, } M_3 \text{ off, and } M_4 \text{ off} \]
\[ \Rightarrow V_o = L \]

\[
\begin{array}{ccc}
  V_A & V_B & V_o \\
  L & L & H \\
  L & H & L \\
  H & L & L \\
  H & H & L \\
\end{array}
\]

This is the NOR truth table.
The CMOS NAND Gate

\[ z = \overline{A \cdot B} = \overline{A} + \overline{B} \]

\[
\begin{array}{c|c|c|c}
A & B & z \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

\[ V_A = L \quad V_B = L \]
\[ \Rightarrow M_1 \text{ off, } M_2 \text{ on, } M_3 \text{ on, and } M_4 \text{ on} \]
\[ \Rightarrow V_o = H \]

\[ V_A = L \quad V_B = H \]
\[ \Rightarrow M_1 \text{ off, } M_2 \text{ on, } M_3 \text{ on, and } M_4 \text{ off} \]
\[ \Rightarrow V_o = H \]

\[ V_A = H \quad V_B = L \]
\[ \Rightarrow M_1 \text{ on, } M_2 \text{ off, } M_3 \text{ off, and } M_4 \text{ on} \]
\[ \Rightarrow V_o = H \]
\[ V_A = H \quad V_B = H \]
\[ \Rightarrow M_1 \text{ on, } M_2 \text{ on, } M_3 \text{ off, and } M_4 \text{ off} \]
\[ \Rightarrow V_0 = L \]

<table>
<thead>
<tr>
<th>( V_A )</th>
<th>( V_B )</th>
<th>( V_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
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<td>H</td>
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</tbody>
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This is the NAND truth table.

The BJT TTL NAND Gate

![NAND Gate Diagram]
For \( V_A = V_B = V^+ \), both DA and DB are OFF. DC is turned on and a voltage is applied to the base of Q2 which saturates Q2, i.e. Q2 becomes almost a short circuit. Its emitter voltage increases, which causes Q4 to saturate. Its collector voltage decreases, which cuts off Q4. In this case \( V_0 \approx 0 \), i.e. \( V_0 = L \).

If either \( V_A = 0 \) or \( V_B = 0 \), then DC is OFF. This cuts off Q2 and Q4. The voltage applied to the base of Q3 saturates it. In this case, \( V_0 \approx V^+ \), i.e. \( V_0 = H \).

Thus the circuit performs the NAND operation. The purpose of DI is to keep Q3 cut off when Q2 and Q4 are saturated.