The FET Bias Equation

Basic Bias Equation

(a) Look out of the 3 MOSFET terminals and replace the circuits with Thévenin equivalent circuits as shown in Fig. 1.

(b) Solve the FET drain current equation for $V_{GS}$.

$$V_{GS} = \sqrt{\frac{I_D}{K}} + V_{TO}$$

(c) Write the gate-source loop equation in the gate-source loop and let $I_S = I_D$.

$$V_{GG} - V_{SS} = V_{GS} + I_S R_{SS} = V_{GS} + I_D R_{SS}$$

(d) Solve the loop equation for $V_{GS}$.

$$V_{GS} = V_{GG} - V_{SS} - I_D R_{SS}$$

(e) Equate the two expressions for $V_{GS}$ and rearrange the terms to obtain a quadratic equation in $\sqrt{I_D}$.

$$I_D R_{SS} + \sqrt{\frac{I_D}{K}} - (V_{GG} - V_{SS} - V_{TO}) = 0$$

(f) Let $a = R_{SS}$, $b = 1/\sqrt{K}$, and $c = - (V_{GG} - V_{SS} - V_{TO})$. In this case, the bias equation becomes

$$a I_D + b \sqrt{I_D} + c = 0$$

Use the quadratic equation to solve for $\sqrt{I_D}$, then square the result to obtain

$$I_D = \left(\frac{-b + \sqrt{b^2 - 4ac}}{2a}\right)^2$$

Note that there is a second solution using the minus sign for the radical. This solution results in $V_{GS} < V_{TO}$, which is a non realizable solution. The desired solution is the one which gives the smaller value of $I_D$.

(e) Check for the active mode. For the active mode, $V_{DS} > V_{GS} - V_{TO} = \sqrt{I_D/K}$.

$$V_{DS} = V_D - V_S = (V_{DD} - I_D R_{DD}) - (V_{SS} + I_S R_{SS}) = V_{DD} - V_{SS} - I_D (R_{DD} + R_{SS})$$
Example 1

\[ V_{GG} = \frac{V^+ R_2 + V^- R_1}{R_1 + R_2} \quad R_{GG} = R_1 || R_2 \]

\[ V_{SS} = V^- \quad R_{SS} = R_S \quad V_{DD} = V^+ \quad R_{DD} = R_D \]

Example 2

\[ V_{GG} = V^+ \frac{R_2}{R_D + R_1 + R_2} - I_D \frac{R_D}{R_D + R_1 + R_2} R_2 \quad R_{GG} = (R_1 + R_D) || R_2 \]

\[ V_{DD} = V^+ \frac{R_1 + R_2}{R_D + R_1 + R_2} \quad R_{DD} = R_D || (R_1 + R_2) \]

\[ V_{SS} = 0 \quad R_{SS} = R_S \]

The gate-source loop equation is

\[ V^+ \frac{R_2}{R_D + R_1 + R_2} - I_D \frac{R_D}{R_D + R_1 + R_2} R_2 = V_{GS} + I_D R_S \]
This can be solved for $V_{GS}$ and equated to $\sqrt{I_D/K} + V_{TO}$ to obtain

$$I_D\left(R_S + \frac{R_D R_2}{R_D + R_1 + R_2}\right) + \sqrt{\frac{I_D}{K}} - \left(\frac{V^+ R_2}{R_D + R_1 + R_2} - V_{TO}\right) = 0$$

The $a$, $b$, and $c$ in the bias equation are given by

$$a = R_S + \frac{R_D R_2}{R_D + R_1 + R_2} \quad b = \frac{1}{\sqrt{K}} \quad c = -\left(\frac{V^+ R_2}{R_D + R_1 + R_2} - V_{TO}\right)$$

Example 3

![Circuit for Example 3](image)

$V_{GG} = \frac{V^+ R_2}{R_1 + R_2}$  $R_{GG} = R_1 || R_2$

$V_{SS} = V^+ - I_D \frac{R_D}{R_D + R_3 + R_S}$  $R_{SS} = R_S || (R_D + R_3)$

$V_{DD} = V^+ \frac{R_3 + R_S}{R_D + R_3 + R_S} + I_S \frac{R_S}{R_D + R_3 + R_S}$  $R_{DD} = R_D || (R_3 + R_S)$

Let $I_S = I_D$. The bias equation for $I_D$ is

$$\frac{V^+ R_2}{R_1 + R_2} - \left(V^+ \frac{R_2}{R_D + R_3 + R_S} - I_D \frac{R_D}{R_D + R_3 + R_S} R_S\right) = \sqrt{\frac{I_D}{K}} + V_{TO} + I_D [R_S || (R_D + R_3)]$$

which gives

$$I_D\left(R_S || (R_D + R_3) - \frac{R_D R_S}{R_D + R_3 + R_S}\right) + \sqrt{\frac{I_D}{K}} - \left(\frac{V^+ R_2}{R_1 + R_2} - \frac{V^+ R_S}{R_D + R_3 + R_S} - V_{TO}\right) = 0$$

The $a$, $b$, and $c$ in the bias equation are given by

$$a = R_S || (R_D + R_3) - \frac{R_D R_S}{R_D + R_3 + R_S} \quad b = \sqrt{\frac{1}{K}}$$

$$c = -\left(\frac{V^+ R_2}{R_1 + R_2} - \frac{V^+ R_S}{R_D + R_3 + R_S} - V_{TO}\right)$$
Example 4

For $M_1$

\[ V_{GG1} = V^+ \frac{R_2}{R_1 + R_2} \quad R_{GG1} = R_1 || R_2 \quad V_{SS1} = 0 \quad R_{SS1} = R_S \]

\[ V_{DD1} = V^+ \quad R_{DD1} = R_D \]

The loop equation for $I_{D1}$ is

\[ V^+ \frac{R_2}{R_1 + R_2} = V_{GS1} + I_{D1} R_S \]

This and the equation for $V_{GS1}$ can be solved for $I_{D1}$.

For $M_2$

\[ V_{GG2} = V^+ - I_{D1} R_D \quad R_{GG2} = R_D \]

\[ V_{SS2} = 0 \quad R_{SS2} = R_S \quad V_{DD2} = V^+ \quad R_{DD2} = R_D \]

The loop equation for $I_{D2}$ is

\[ V^+ - I_{D1} R_D = V_{GS2} + I_{D2} R_S \]

This and the equation for $V_{GS2}$ can be solve for $I_{D2}$.

Given $I_{D1}$ and $I_{D2}$, it can be determined if the two MOSFETs are in the active mode.

Example 5

\[ V_{GG1} = V^+ \frac{R_2}{R_1 + R_2} \quad R_{GG1} = R_1 || R_2 \quad V_{SS1} = 0 \quad R_{SS1} = R_S \]

\[ V_{GG2} = I_S R_S \quad R_{GG2} = R_S \quad V_{SS2} = 0 \quad R_{SS2} = R_S \quad V_{DD2} = V^+ \quad R_{DD2} = R_D \]

Let the currents to be solved be $I_{D1}$ and $I_{D2}$ and let $I_S = I_{D1}$ and $I_S = I_{D2}$.

The gate-source loop equation for $I_{D1}$ is

\[ V^+ \frac{R_2}{R_1 + R_2} = V_{GS1} + I_{D1} R_S \]

This and the equation for $V_{GS1}$ can be solved for $I_{D1}$.

The gate-source loop equation for $I_{D2}$ is

\[ I_{D1} R_S = V_{GS2} + I_{D2} R_S \]

Given $I_{D1}$ and $I_{D2}$, it can be determined if the two MOSFETs are in the active mode.
Figure 6: Circuit for Example 5.