The MOSFET

Device Equations

Whereas the JFET has a diode junction between the gate and the channel, the metal-oxide semiconductor FET or MOSFET differs primarily in that it has an oxide insulating layer separating the gate and the channel. The circuit symbols are shown in Fig. 1. Each device has gate (G), drain (D), and source (S) terminals. Four of the symbols show an additional terminal called the body (B) which is not normally used as an input or an output. It connects to the drain-source channel through a diode junction. In discrete MOSFETs, the body lead is connected internally to the source. When this is the case, it is omitted on the symbol as shown in four of the MOSFET symbols. In integrated-circuit MOSFETs, the body usually connects to a dc power supply rail which reverse biases the body-channel junction. In the latter case, the so-called "body effect" must be accounted for when analyzing the circuit.

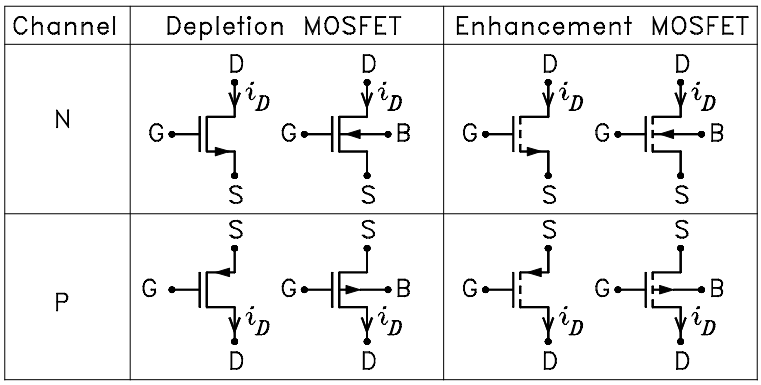

Figure 1: MOSFET symbols.

The discussion here applies to the n-channel MOSFET. The equations apply to the p-channel device if the subscripts for the voltage between any two of the device terminals are reversed, e.g. v_{GS} becomes v_{SG}. The n-channel MOSFET is biased in the active mode or saturation region for $v_{DS} \geq v_{GS} - v_{TH}$, where v_{TH} is the threshold voltage. This voltage is negative for the depletion-mode device and positive for the enhancement-mode device. It is a function of the body-source voltage and is given by

$$v_{TH} = V_{TO} + \gamma \left[\sqrt{\phi - v_{BS}} - \sqrt{\phi} \right] \tag{1}$$

where V_{TO} is the value of v_{TH} with $v_{BS} = 0$, γ is the body threshold parameter, ϕ is the surface potential, and v_{BS} is the body-source voltage. The drain current is given by

$$i_D = \frac{k'}{2} \frac{W}{L} (1 + \lambda v_{DS}) (v_{GS} - v_{TH})^2 \tag{2}$$

where W is the channel width, L is the channel length, λ is the channel-length modulation parameter, and k' is given by

$$k' = \mu_0 C_{ox} = \mu \frac{\epsilon_{ox}}{t_{ox}}$$

In this equation, μ_0 is the average carrier mobility, C_{ox} is the gate oxide capacitance per unity area, ϵ_{ox} is the permittivity of the oxide layer, and t_{ox} is its thickness. It is convenient to define a transconductance coefficient K given by

$$K = \frac{k'}{2} \frac{W}{L} (1 + \lambda v_{DS}) \tag{3}$$

With this definition, the drain current can be written

$$i_D = K\left(v_{GS} - v_{TH}\right)^2 \tag{4}$$

Note that K plays the same role in the MOSFET drain current equation as β plays in the JFET drain current equation.

Figure 2 shows the typical variation of drain current with gate-to-source voltage for a constant drain-to-source voltage and zero body-to-source voltage. In this case, the threshold voltage is a constant, i.e. $v_{TH} = V_{TO}$. For $v_{GS} \leq V_{TO}$, the drain current is zero. For $v_{GS} > V_{TO}$, the drain current increases approximately as the square of the gate-to-source voltage. The slope of the curve represents the small-signal transconductance g_m, which is defined in the next section. Fig. 3 shows the typical variation of drain current with drain-to-source voltage for a several values of gate-to-source voltage v_{GS} and zero body-to-source voltage v_{BS}. The dashed line divides the triode region from the saturation or active region. In the saturation region, the slope of the curves represents the reciprocal of the small-signal drain-source resistance r_0, which is defined in the next section.

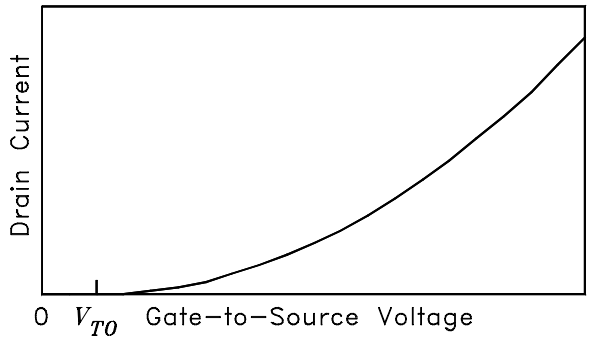

Figure 2: Drain current i_D versus gate-to-source voltage v_{GS} for constant drain-to-source voltage v_{DS}.

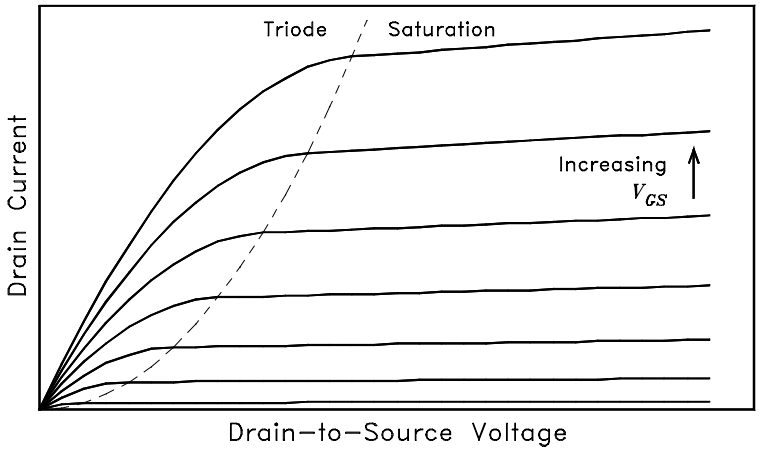

Figure 3: Drain current i_D versus drain-to-source voltage v_{DS} for constant gate-to-source voltage v_{GS}.

Bias Equation

Figure 4 shows the MOSFET with the external circuits represented by Thévenin dc circuits. If the MOSFET is in the pinch-off region, the following equations for I_D hold:

$$I_D = K\left(V_{GS} - V_{TH}\right)^2 \tag{5}$$

$$V_{GS} = V_{GG} - (V_{SS} + I_D R_{SS}) \tag{6}$$

$$K = K_0 \left(1 + \lambda V_{DS}\right) \tag{7}$$

$$V_{DS} = (V_{DD} - I_D R_{DD}) - (V_{SS} + I_D R_{SS}) \tag{8}$$

Because this is a set of nonlinear equations, a closed form solution for I_D cannot be easily written unless it is assumed that K is not a function of V_{DS} and V_{TH} is not a function of V_{BS}. The former assumption requires the condition $\lambda V_{DS} \ll 1$. With these assumptions, the equations can be solved for I_D to obtain

$$I_D = \frac{1}{4KR_{SS}^2}\left[\sqrt{1 + 4KR_{SS}\left(V_{GG} - V_{SS} - V_{TH}\right)} - 1\right]^2 \tag{9}$$

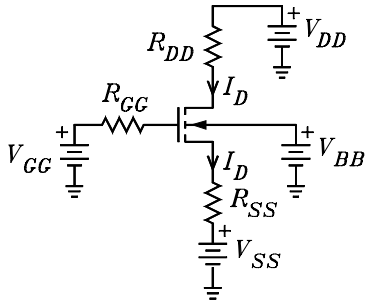

Figure 4: MOSFET dc bias circuit.

Unless $\lambda V_{DS} \ll 1$ and the dependence of V_{TH} on V_{BS} is neglected, Eq. (9) is only an approximate solution. A numerical procedure for obtaining a more accurate solution is to first calculate I_D with $K = K_0$ and $V_{TH} = V_{TO}$. Then calculate V_{DS} and the new values of K and V_{TH} from which a new value for I_D can be calculated. The procedure can be repeated until the solution for I_D converges. Alternately, computer tools can be used to obtain a numerical solution to the set of nonlinear equations.

Small-Signal Models

There are two small-signal circuit models which are commonly used to analyze MOSFET circuits. These are the hybrid-π model and the T model. The two models are equivalent and give identical results. They are described below.

Hybrid-π Model

Let the drain current and each voltage be written as the sum of a dc component and a small-signal ac component as follows:

$$i_D = I_D + i_d \tag{10}$$

$$v_{GS} = V_{GS} + v_{gs} \tag{11}$$

$$v_{BS} = V_{BS} + v_{bs} \tag{12}$$

$$v_{DS} = V_{DS} + v_{ds} \tag{13}$$

If the ac components are sufficiently small, we can write

$$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{BS}} v_{bs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} \tag{14}$$

where the derivatives are evaluated at the dc bias values. Let us define

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = K\left(V_{GS} - V_{TH}\right) = 2\sqrt{KI_D} \tag{15}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\gamma\sqrt{KI_D}}{\sqrt{\phi - V_{BS}}} = \chi g_m \tag{16}$$

$$\chi = \frac{\gamma}{2\sqrt{\phi - V_{BS}}} \tag{17}$$

$$r_0 = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1} = \left[\frac{k'}{2}\frac{W}{L}\lambda\left(V_{GS} - V_{TH}\right)^2\right]^{-1} = \frac{V_{DS} + 1/\lambda}{I_D} \tag{18}$$

The small-signal drain current can thus be written

$$i_d = i_{dg} + i_{db} + \frac{v_{ds}}{r_0} \tag{19}$$

where

$$i_{dg} = g_m v_{gs} \tag{20}$$

$$i_{db} = g_{mb} v_{bs} \tag{21}$$

The small-signal circuit which models these equations is given in Fig. 5. This is called the hybrid-π model.

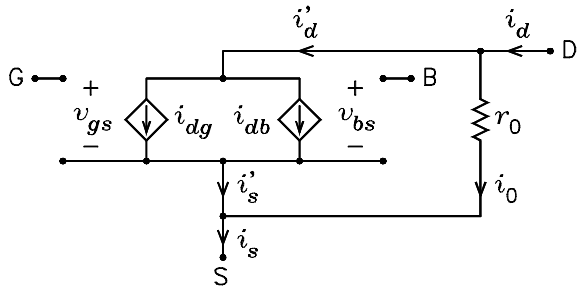

Figure 5: Hybrid-π model of the MOSFET.

T Model

The T model of the MOSFET is shown in Fig. 6. The resistor r_0 is given by Eq. (18). The resistors r_s and r_{sb} are given by

$$r_s = \frac{1}{g_m} \tag{22}$$

$$r_{sb} = \frac{1}{g_{mb}} = \frac{1}{\chi g_m} = \frac{r_s}{\chi} \tag{23}$$

where g_m and g_{mb} are the transconductances defined in Eqs. (15) and (16). The currents are given by

$$i_d = i_{sg} + i_{sb} + \frac{v_{ds}}{r_0} \tag{24}$$

$$i_{sg} = \frac{v_{gs}}{r_s} = g_m v_{gs} \tag{25}$$

$$i_{sb} = \frac{v_{bs}}{r_{sb}} = g_{mb} v_{bs} \tag{26}$$

The currents are the same as for the hybrid-π model. Therefore, the two models are equivalent. Note that the gate and body currents are zero because the two controlled sources supply the currents that flow through r_s and r_{sb}.

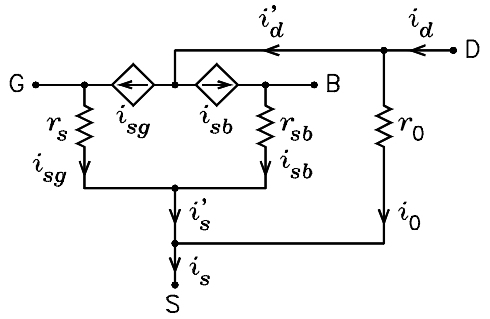

Figure 6: T model of the MOSFET.

Small-Signal Equivalent Circuits

Several equivalent circuits are derived below which facilitate writing small-signal low-frequency equations for the MOSFET. We assume that the circuits external to the device can be represented by Thévenin equivalent circuits. The Norton equivalent circuit seen looking into the drain and the Thévenin equivalent circuit seen looking into the source are derived. Several examples are given which illustrate use of the equivalent circuits.

Simplified T Model

Figure 7 shows the MOSFET T model with a Thévenin source in series with the gate and the body connected to signal ground. We wish to solve for the equivalent circuit in which the sources i_{sg} and i_{sb} are replaced by a single source which connects from the drain node to ground having the value $i'_d = i'_s$. We call this the simplified T model. The first step is to look up into the branch labeled i'_s and form a Thévenin equivalent circuit. With $i'_s = 0$, we can use voltage division to write

$$v_{s(oc)} = v_{tg}\frac{r_{sb}}{r_s + r_{sb}} = v_{tg}\frac{r_s/\chi}{r_s + r_s/\chi} = \frac{v_{tg}}{1+\chi} \tag{27}$$

With $v_{tg} = 0$, the resistance r'_s seen looking up into the branch labeled i'_s is

$$r'_s = r_s \| r_{sb} = \frac{r_s}{1+\chi} = \frac{1}{(1+\chi)\, g_m} \tag{28}$$

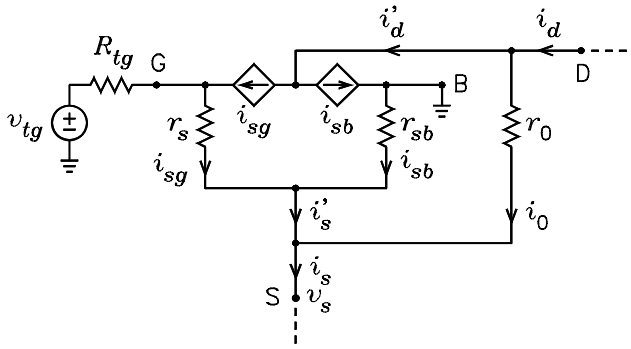

Figure 7: T model with Thévenin source connected to the gate and the body connected to signal ground.

The simplified T model is shown in Fig.8. Compared to the corresponding circuit for the BJT, the MOSFET circuit replaces v_{tb} with $v_{tg}/(1+\chi)$ and r'_e with $r'_s = r_s/(1+\chi)$. Because the gate current is zero, set $\alpha = 1$ and $\beta = \infty$ in converting any BJT formulas to corresponding MOSFET formulas. The simplified T model is derived with the assumption that the body lead connects to signal ground. In the case

that the body lead connects to the source lead, it follows from Fig. 7 that $i_{sb} = 0$. Connecting the body to the source is equivalent to setting $\chi = 0$ in the MOSFET equations.

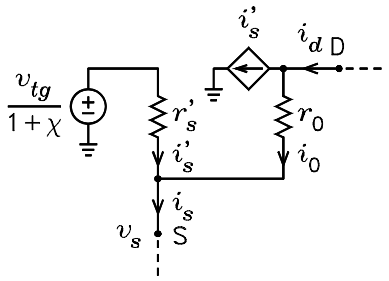

Figure 8: Simplified T model.

Norton Drain Circuit

Figure 9(a) shows the MOSFET with Thévenin sources connected to its gate and source leads and the body lead connected to signal ground. The Norton equivalent circuit seen looking into the drain can be obtained from the Norton equivalent circuit seen looking into the BJT collector by replacing G_{mb} with G_{mg}, G_{me} with G_{ms}, and r_{ic} with r_{id}. The factor $1/(1+\chi)$ must be incorporated into the equation for G_{mg}. To convert the formulas, replace R_{tb} with R_{tg}, R_{te} with R_{te}, R_{tc} with R_{td}, r'_e with r'_s, set $\alpha = 1$, and set $\beta = \infty$. The circuit is given in Fig. 9(b), where $i_{d(sc)}$ and r_{id} are given by

$$i_{d(sc)} = G_{mg} v_{tg} - G_{ms} v_{ts} \tag{29}$$

$$r_{id} = r_0 \left(1 + \frac{R_{ts}}{r'_s}\right) + R_{ts} \tag{30}$$

The transconductances G_{mg} and G_{ms} are given by

$$G_{mg} = \frac{1}{1+\chi} \frac{1}{r'_s + R_{ts} \| r_0} \frac{r_0}{r_0 + R_{ts}} \tag{31}$$

$$G_{ms} = \frac{1}{R_{ts} + r'_s \| r_0} \tag{32}$$

The equations for the case where the body is connected to the source are obtained by setting $\chi = 0$. For the case $R_{ts} = 0$, the equations for G_{mg} and G_{ms} reduce to

$$G_{mg} = \frac{1}{1+\chi} \frac{1}{r'_s} = g_m \tag{33}$$

$$G_{ms} = \frac{1}{r'_s \| r_0} = (1+\chi)\, g_m + \frac{1}{r_0} \tag{34}$$

For the case $r_0 \gg R_{ts}$ and $r_0 \gg r'_s$, we can write

$$G_{mg} = \frac{1}{1+\chi} \frac{1}{r'_s + R_{ts}} \tag{35}$$

and

$$G_{ms} = \frac{1}{r'_s + R_{ts}} \tag{36}$$

The value of $i_{d(sc)}$ calculated with these approximations is simply the value of i'_s calculated with r_0 considered to be an open circuit. The term "r_0 approximations" is used in the following when r_0 is neglected in calculating $i_{d(sc)}$ but not neglected in calculating r_{id}.

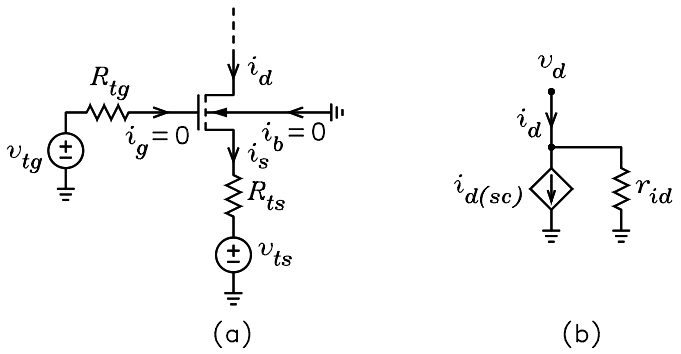

Figure 9: (a) MOSFET with Thévenin sources connected to the gate and source. (b) Norton drain circuit.

Thévenin Source Circuit

Figure 10(a) shows the MOSFET with a Thévenin source connected to its gate, the body lead connected to signal ground, and the external drain load represented by the resistor R_{td}. The Thévenin equivalent circuit seen looking into the source can be obtained from the Thévenin equivalent circuit seen looking into the BJT emitter by replacing $v_{e(oc)}$ with $v_{s(oc)}$, r_{ie} with r_{is}, v_{tb} with $v_{tg}/(1+\chi)$, R_{tb} with R_{tg}, R_{tc} with R_{td}, r'_e with r'_s, setting $\alpha = 1$, and setting $\beta = \infty$. The circuit is given in Fig. 10(b), where $v_{s(oc)}$ and r_{is} are given by

$$v_{s(oc)} = \frac{v_{tg}}{1+\chi}\,\frac{r_0}{r_0 + r'_s} \tag{37}$$

$$r_{is} = r'_s\frac{r_0 + R_{td}}{r_0 + r'_s} \tag{38}$$

The equations for the case where the body is connected to the source are obtained by setting $\chi = 0$.

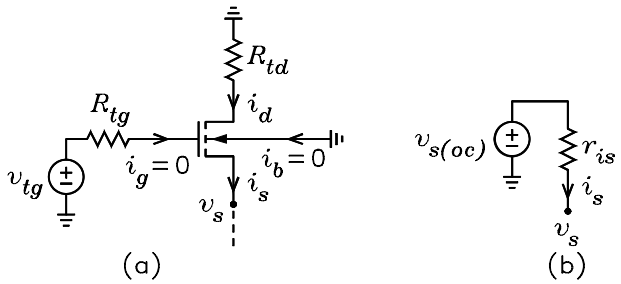

Figure 10: (a) MOSFET with Thévenin source connected to gate. (b) Thévenin source circuit.

The r_0 Approximations

The r_0 approximations approximate r_0 as an open circuit in all equations except the one for r_{id}. In this case, the equations for $i_{d(sc)}$, G_{mg}, G_{ms}, r_{id}, $v_{s(oc)}$, and r_{is} are

$$i_{d(sc)} = i'_d = G_{mg}v_{tg} - G_{ms}v_{ts} \qquad G_{mg} = \frac{1}{1+\chi}\,\frac{1}{r'_s + R_{ts}} \qquad G_{ms} = \frac{1}{r'_s + R_{ts}} \tag{39}$$

$$r_{id} = \frac{r_0 + r'_s \| R_{ts}}{1 - R_{ts}/(r'_s + R_{ts})} \overset{\text{or}}{=} r_0\left(1 + \frac{R_{ts}}{r'_s}\right) + R_{ts} \tag{40}$$

$$v_{e(oc)} = \frac{v_{tg}}{1+\chi} \qquad r_{is} = r'_s \tag{41}$$

The simplified T model, the hybrid π model, and the T model, respectively, are given Figs. 11 - 13. If $r_0 = \infty$, then r_{id} is an open circuit in each. Because r_0 no longer connects to the source, there is only one source current and $i_s = i'_s$.

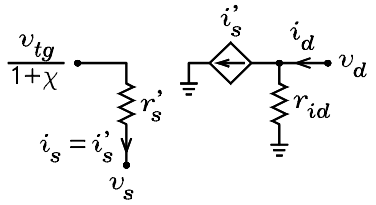

Figure 11: Simplified T model with r_0 approximations.

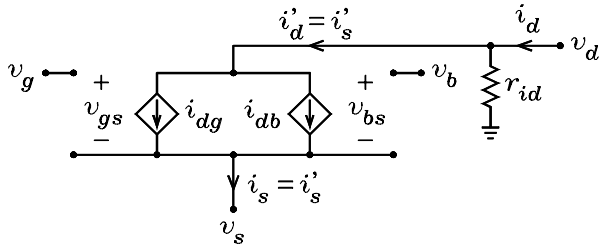

Figure 12: Hybrid π model with the r_0 approximations.

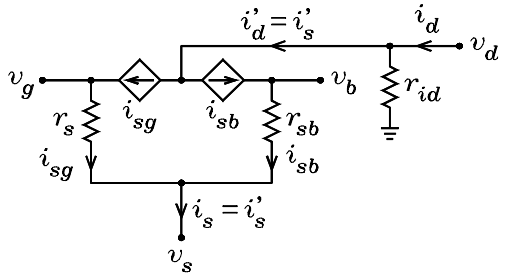

Figure 13: T model with the r_0 approximations.

Summary of Models

Figure 14 summarizes the four equivalent circuits derived above. For the case where the body is connected to the source, set $\chi = 0$ in the equations.

Example Amplifier Circuits

This section describes several examples which illustrate the use of the small-signal equivalent circuits derived above to write by inspection the voltage gain, the input resistance, and the output resistance of several amplifier circuits.

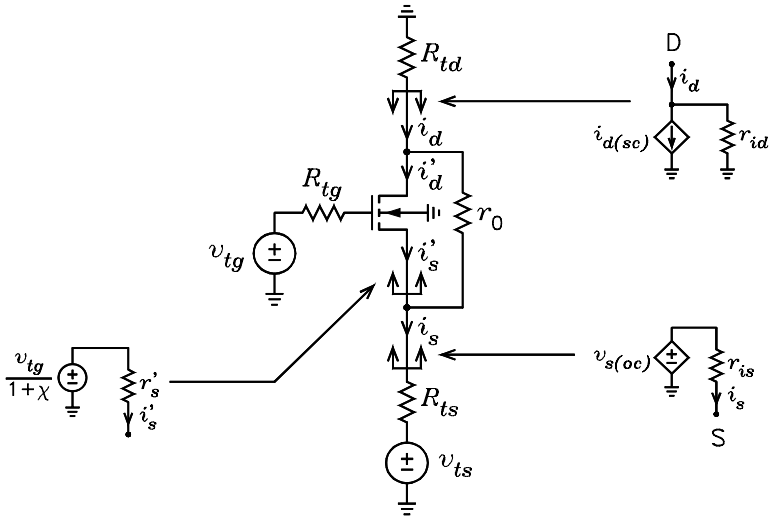

Figure 14: Summary of the small-signal equivalent circuits. Set $\chi = 0$ if the body is connected to the source.

Common-Source Amplifier

Figure 15(a) shows a common-source amplifier. The active device is M_1. Its load consists of a current-mirror active load consisting of M_2 and M_3. The current source I_Q sets the drain current in M_3 which is mirrored into the drain of M_2. Because the source-to-drain voltage of M_2 is larger than that of M_3, the Early effect causes the dc drain current in M_2 to be slightly larger than I_Q. The input voltage can be written $v_I = V_B + v_i$, where V_B is a dc bias voltage which sets the drain current in M_1. It must be equal to the drain current in M_2 in order for the dc component of the output voltage to be stable. In any application of the circuit, V_B would be set by feedback. Looking out of the drain of M_1, the resistance to ac signal ground is $R_{td1} = r_{02}$.

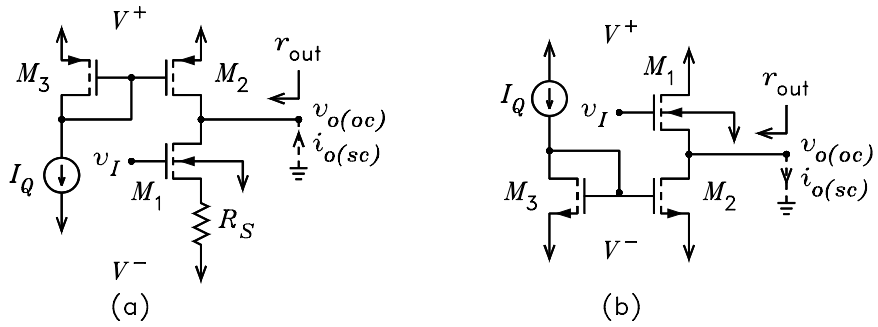

Figure 15: (a) CMOS common-source amplifier. (b) Common-drain amplifier.

The voltage gain of the circuit can be written

$$\frac{v_o}{v_i} = \frac{i_{d1(sc)}}{v_i} \frac{v_o}{i_{d1(sc)}} = G_{mg1} \times (-r_{id1} \| r_{02}) \tag{42}$$

where G_{mg1} is given by Eq. (31), r_{id1} is given by Eq. (30), and $R_{ts1} = R_S$. The body effect cancels if $R_S = 0$. The output resistance is given by

$$r_{out} = r_{id1} \| r_{02} \tag{43}$$

Common-Drain Amplifier

Figure 15(b) shows a common-drain amplifier. The active device is M_1. Its load consists of a current-mirror active load consisting of M_2 and M_3. The current source I_Q sets the drain current in M_3 which is mirrored into the drain of M_2. As with the common-source amplifier, the Early effect makes the drain current in M_2 slightly larger than that in M_3. The input voltage can be written $v_I = V_B + v_i$, where V_B is a dc bias voltage which sets the dc component of the output voltage. Looking out of the source of M_1, the resistance to ac signal ground is $R_{ts1} = r_{02}$. The voltage gain can be written

$$\frac{v_o}{v_i} = \frac{v_{s1(oc)}}{v_i}\,\frac{v_o}{v_{s1(oc)}} = \frac{1}{1+\chi_1}\,\frac{r_{01}}{r_{01}+r'_{s1}}\,\frac{r_{02}}{r_{02}+r_{is1}} \tag{44}$$

where $r_{is1}$is given by Eq. (38). The output resistance is given by

$$r_{out} = r_{is1} \| r_{02} \tag{45}$$

Common-Gate Amplifier

Figure 16(a) shows a common-gate amplifier. The active device is M_1. Its load consists of a current-mirror active load consisting of M_2 and M_3. The current source I_Q sets the drain current in M_3 which is mirrored into the drain of M_2. As with the common-source amplifier, the Early effect makes the drain current in M_2 slightly larger than that in M_3. The dc voltage V_B is a dc bias voltage which sets the drain current in M_1 which must be equal to the drain current in M_2 in order for the dc component of the output voltage to be stable. In any application of the circuit, V_B would be set by feedback. Looking out of the drain of M_1, the resistance to ac signal ground is $R_{td1} = r_{02}$.

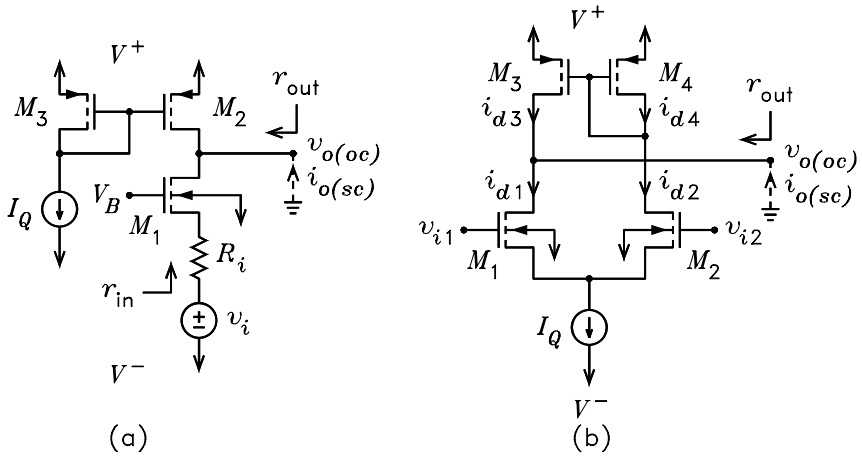

Figure 16: (a) CMOS Common-gate amplifier. (b) CMOS differential amplifier.

The voltage gain of the circuit can be written

$$\frac{v_o}{v_i} = \frac{i_{d1(sc)}}{v_i}\,\frac{v_0}{i_{d1(sc)}} = -G_{ms1} \times (-r_{id1} \| r_{02}) \tag{46}$$

where G_{ms1} is given by Eq. (32) and r_{id1} is given by Eq. (30). The input and output resistances are given by

$$r_{in} = R_i + r_{is1} \tag{47}$$

$$r_{out} = r_{id1} \| r_{02} \tag{48}$$

where $r_{is1}$is given by Eq. (38).

Differential Amplifier

A MOS differential amplifier with an active current-mirror load is shown in Fig. 16(b). The object is to determine the Norton equivalent circuit seen looking into the output To do this, the output is connected to ac signal ground, which is indicated by the dashed line. It will be assumed that the Early effect can be neglected in all devices in calculating $i_{o(sc)}$ but not neglected in calculating r_{out}, i.e. we use the r_0 approximations. We can write

$$i_{o(sc)} = i_{d1(sc)} - i_{d3(sc)} = i_{d1(sc)} - i_{d4(sc)} = i_{d1(sc)} - i_{d2(sc)} \tag{49}$$

Because the tail supply is a current source, the currents i_{d1} and i_{d2} can be calculated by replacing v_{i1} and v_{i2} with their differential components. In this case, the ac signal voltage at the sources of M_1 and M_2 is zero. Let $v_{i1} = v_{i(d)}/2$ and $v_{i2} = -v_{i(d)}/2$, where $v_{id} = v_{i1} - v_{i2}$. It follows by symmetry that $i_{d2(sc)} = -i_{d1(sc)}$ so that $i_{o(sc)}$ is given by

$$\begin{aligned} i_{o(sc)} &= 2i_{d1(sc)} = 2G_{mg1}\frac{v_{i(d)}}{2} \\ &= 2\frac{1}{(1+\chi)}\frac{1}{r'_s}\frac{v_{i(d)}}{2} = g_{m1}\left(v_{i1} - v_{i2}\right) \end{aligned} \tag{50}$$

where Eq. (35) with $R_{ts} = 0$ is used for G_{mg}. Note that the body effect cancels. This is because the source-to-body ac signal voltage is zero for the differential input signals. The output resistance is given by

$$r_{out} = r_{01} \| r_{03} \tag{51}$$

Note that $r_{id1} = r_{01}$ because $R_{ts1} = R_{ts2} = 0$ for the differential input signals.

Small-Signal High-Frequency Models

Figures 17 and 18 show the hybrid-π and T models for the MOSFET with the gate-source capacitance c_{gs}, the source-body capacitance c_{sb}, the drain-body capacitance c_{db}, the drain-gate capacitance c_{dg}, and the gate-body capacitance c_{gb}added. These capacitors model charge storage in the device which affect its high-frequency performance. The first three capacitors are given by

$$c_{gs} = \frac{2}{3}WLC_{ox} \tag{52}$$

$$c_{sb} = \frac{c_{sb0}}{\left(1 + V_{SB}/\psi_0\right)^{1/2}} \tag{53}$$

$$c_{db} = \frac{c_{db0}}{\left(1 + V_{DB}/\psi_0\right)^{1/2}} \tag{54}$$

where V_{SB} and V_{DB} are dc bias voltages; c_{sb0} and c_{db0} are zero-bias values; and ψ_0 is the built-in potential. Capacitors c_{gd} and c_{gb} model parasitic capacitances. For IC devices, c_{gd} is typically in the range of 1 to 10 fF for small devices and c_{gb} is in the range of 0.04 to 0.15 fF per square micron of interconnect.

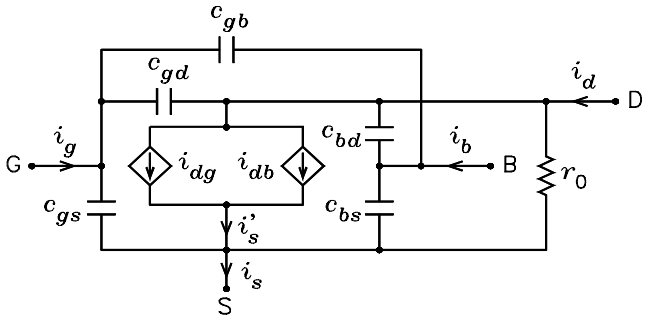

Figure 17: High-frequency hybrid-π model.

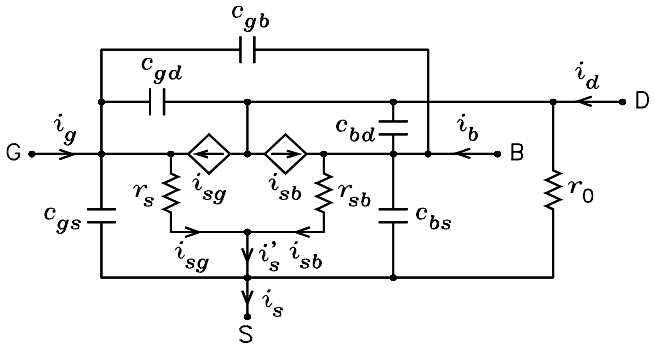

Figure 18: High-frequency T model.