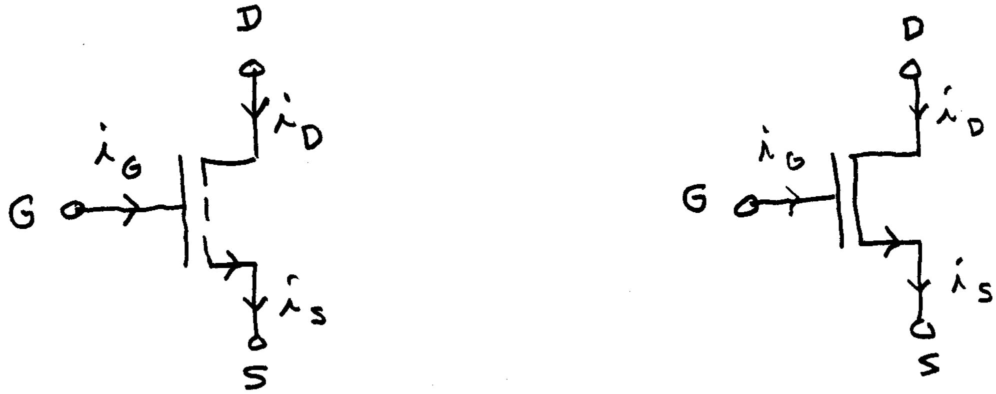
1-05/21/03

The MOSFET

Enhancement Device   Depletion Device



For either device, the drain current is given by

$$i_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (1 + \lambda v_{DS})(v_{GS} - V_{TO})^2$$

μ = majority carrier mobility

C_{ox} = gate oxide capacitance per unit area

W = channel width

L = channel length

λ = channel length modulation parameter (reciprocal of the Early voltage)

V_{TO} = threshold voltage

It is common to define K' as

$$K' = \mu C_{ox}$$

so that i_D can be written

$$i_D = \frac{K'}{2} \frac{W}{L} (1 + \lambda v_{DS})(v_{GS} - V_{TO})^2$$

This equation assumes the active or saturation mode. For the device to be in this mode, we must have

$$v_{DS} > v_{GS} - V_{TO}$$

For the enhancement mode device $V_{TO} > 0$. For the depletion mode device, $V_{TO} < 0$.

To simplify the equation for i_D, let us define

$$K_o = \frac{K'}{2} \frac{W}{L}$$

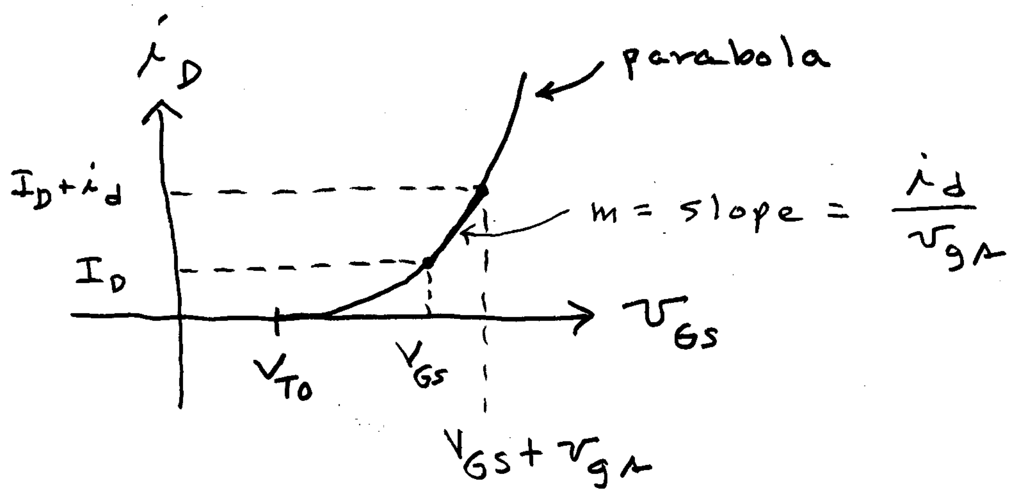
$$K = K_o (1 + \lambda v_{DS})$$

$$\Rightarrow \quad i_D = K (v_{GS} - V_{TO})^2$$

Because the gate is insulated, $i_G = 0$. Thus $i_S = i_D$.

The MOSFET Transfer Characteristics

The transfer characteristics are plots of i_D versus v_{GS} for v_{DS} = constant. Let us assume an enhancement mode device for which $V_{TO} > 0$.



Draw a tangent line at the point (V_{GS}, I_D). The slope of the line can be used to relate changes in i_D to changes in v_{GS}.

$$m = \frac{\partial I_D}{\partial V_{GS}} = 2K\,(V_{GS} - V_{TO})$$

$$= 2K\sqrt{\frac{I_D}{K}}$$

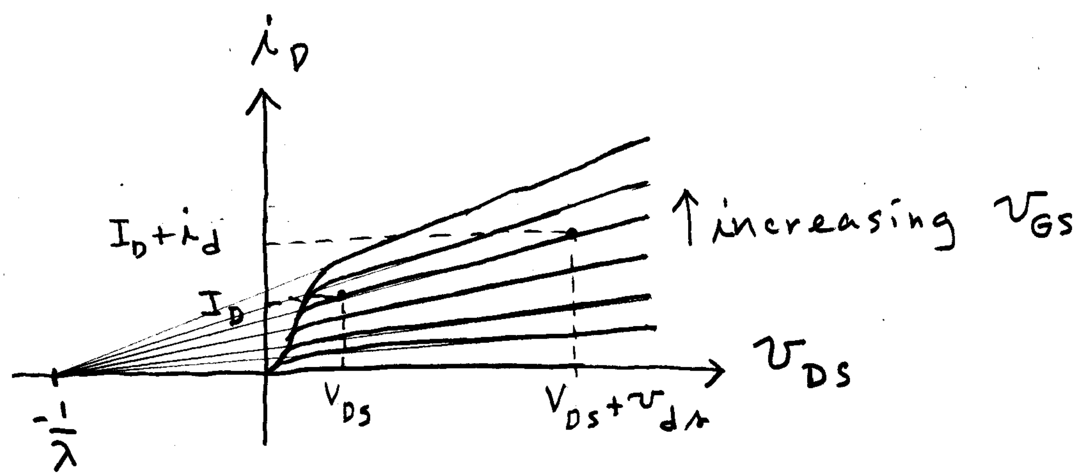
$$= 2\sqrt{K I_D}$$

$$\Rightarrow \quad i_d = 2\sqrt{K I_D}\; v_{gs}$$

The MOSFET Output Characteristics

The output characteristics are plots of i_D versus v_{DS} for v_{GS} = constant.

$$i_D = K_o (1 + \lambda v_{DS})(v_{GS} - V_{TO})^2$$



Draw a tangent line at the point (V_{DS}, I_D). The slope of the line can be used to relate changes in i_D to changes in v_{DS}.

$$m = \frac{\partial I_D}{\partial V_{DS}} = K_o \lambda (V_{GS} - V_{TO})^2$$

$$= \lambda \frac{I_D}{1+\lambda V_{DS}} = \frac{I_D}{\frac{1}{\lambda} + V_{DS}}$$

$$\Rightarrow i_d = \frac{I_D}{\frac{1}{\lambda} + V_{DS}} v_{ds}$$

Thus, in general, we have

$$i_d = 2\sqrt{K I_D}\, v_{gs} + \frac{I_D}{\frac{1}{\lambda} + V_{DS}} v_{ds}$$

Let us define

$$g_m = 2\sqrt{K I_D} \qquad r_o = \frac{\frac{1}{\lambda} + V_{DS}}{I_D}$$

$$\Rightarrow i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$$

Because the gate is insulated, it follows that

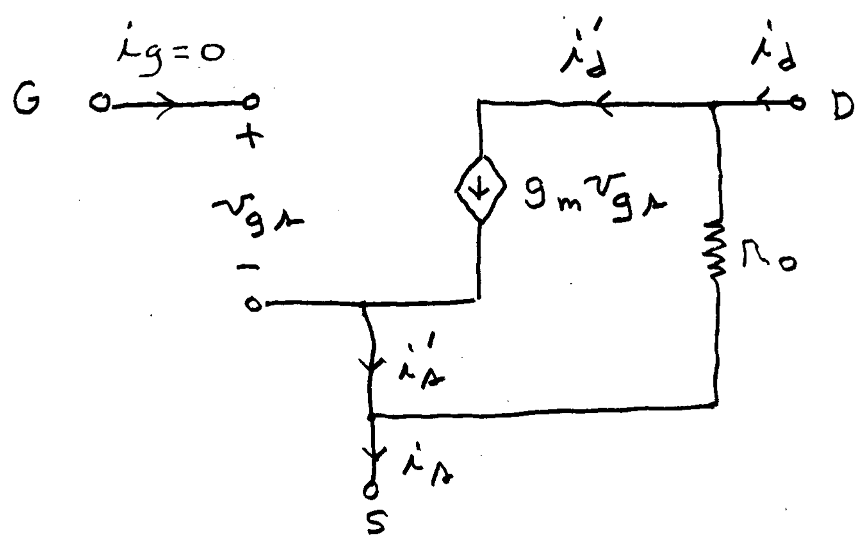
$$i_g = 0 \qquad i_s = i_g + i_d = i_d$$

The Hybrid-π Model

The basic equations are

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o} \qquad i_g = 0$$

We can draw the model as follows:



The T Model

The T model puts a resistor in series with the i_s' branch which has the same voltage across it as v_{gs} in the hybrid-π model.

We can write

$$i_s' = i_d' = g_m v_{gs}$$

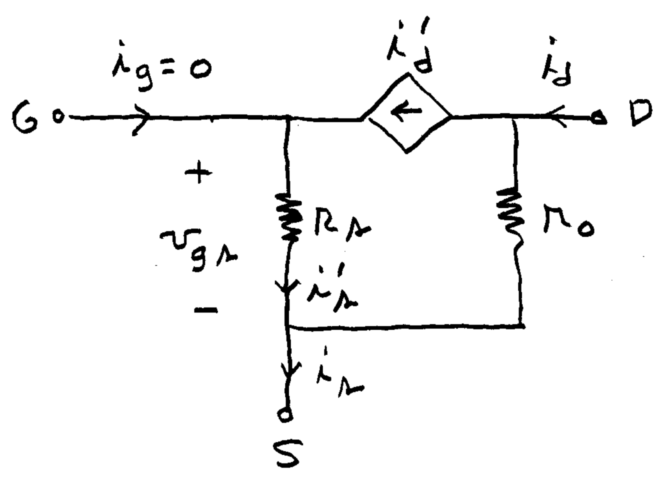
$$\Rightarrow \quad v_{gs} = i_s' \frac{1}{g_m}$$

Let us define the resistance

$$r_s = \frac{1}{g_m}$$

$$\Rightarrow \quad v_{gs} = i_s' r_s$$

Thus the T model is



$$i_d' = i_s' = \frac{v_{gs}}{r_s} = g_m v_{gs}$$

Thus i_d' and i_s' are the same

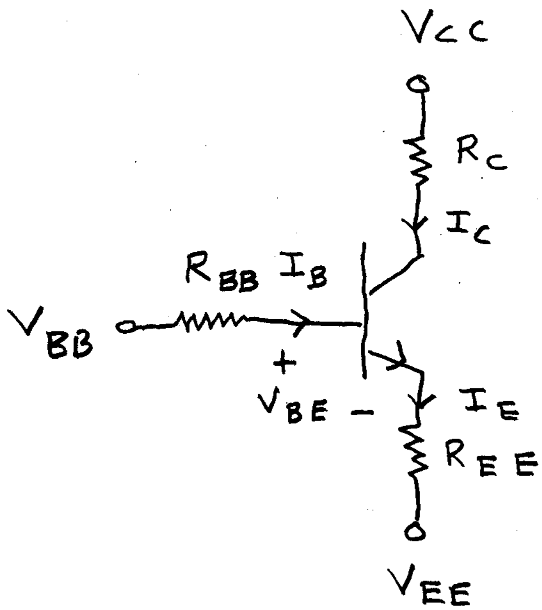
as for the hybrid-π model. Also $i_g = i'_s - i'_d = 0$ which is the same as for the hybrid-π model.

BJT/MOSFET Comparison

	BJT	MOSFET
r_x	> 0	$= 0$
g_m	I_C/V_T	$2\sqrt{KI_D}$
r_π	V_T/I_B	∞
r_0	$\dfrac{V_A + V_{CE}}{I_C}$	$\dfrac{\frac{1}{\lambda} + V_{DS}}{I_D}$
β	I_C/I_B	∞
α	I_C/I_E	1
	$r_e = V_T/I_E$	$r_s = 1/g_m$

The BJT Bias Equation

Replace the dc circuits looking out of the collector, base, and emitter leads with Thévenin equivalents.



The loop equation between the V_{BB} and V_{EE} nodes is

$$V_{BB} - V_{EE} = I_B R_{BB} + V_{BE} + I_E R_{EE}$$

Suppose we desire I_C. We use

$$I_B = \frac{I_C}{\beta} \qquad I_E = \frac{I_C}{\alpha}$$

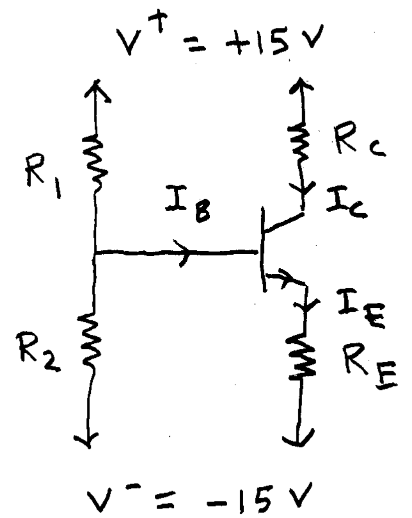
$$\Rightarrow \quad V_{BB} - V_{EE} = I_C \frac{R_{BB}}{\beta} + V_{BE} + I_C \frac{R_{EE}}{\alpha}$$

$$\Rightarrow \quad I_C = \frac{V_{BB} - V_{EE} - V_{BE}}{\frac{R_{BB}}{\beta} + \frac{R_{EE}}{\alpha}}$$

In a similar way, we obtain for I_E

$$I_E = \frac{V_{BB} - V_{EE} - V_{BE}}{\frac{R_{BB}}{1+\beta} + R_{EE}}$$

Example 1



$R_1 = 100\ K\Omega$

$R_2 = 120\ K\Omega$

$R_E = 5.6\ K\Omega$

$\beta = 99$

$\alpha = \frac{\beta}{1+\beta} = 0.99$

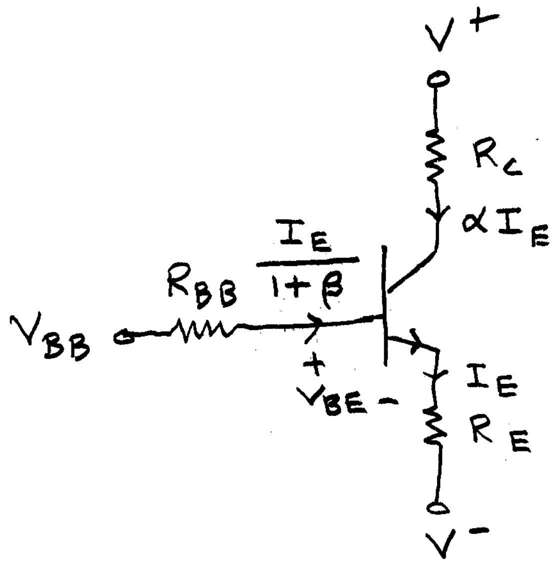
$V_{BE} = 0.65\ V$

Solve for I_E

$$V_{BB} = V^{+} \frac{R_2}{R_1 + R_2} + V^{-} \frac{R_1}{R_1 + R_2} = 1.3636\ V$$

$$R_{BB} = R_1 \| R_2 = 54.45\ k\Omega$$

The equivalent circuit is



$$V_{BB} - V^- = \frac{I_E}{1+\beta} R_{BB} + V_{BE} + I_E R_E$$

$$\Rightarrow \quad I_E = \frac{V_{BB} - V^- - V_{BE}}{\frac{R_{BB}}{1+\beta} + R_E} = 2.557 \text{ mA}$$

Our solution assumes the active mode. This requires $V_{CB} > 0$.

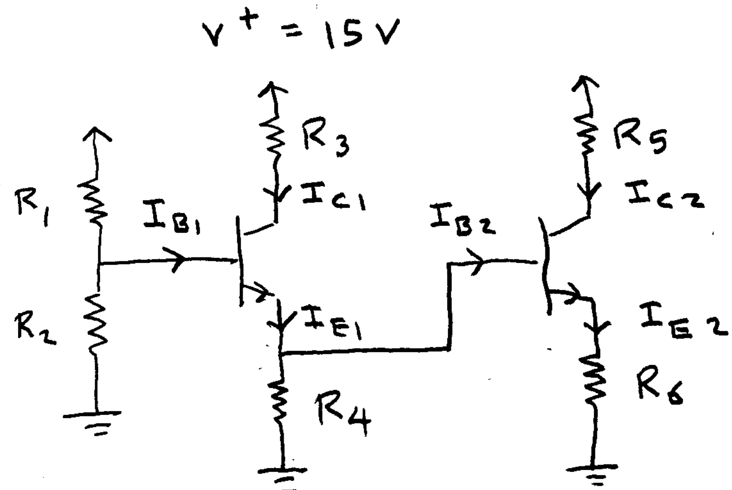
$$V_C = V^+ - \alpha I_E R_C = 4.1151 \text{ V}$$

$$V_B = V_E + V_{BE} = V^- + I_E R_E + V_{BE} = -0.0311 \text{ V}$$

$\Rightarrow \quad V_{CB} = V_C - V_B = 4.1461 \text{ V}$

Because $V_{CB} > 0$, the BJT is in the active mode.

Example 2



$R_1 = 20\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$, $R_3 = R_4 = 3\text{ k}\Omega$

$R_5 = R_6 = 2\text{ k}\Omega$, $V_{BE1} = V_{BE2} = 0.65 \text{ V}$

$\beta_1 = \beta_2 = 100$, $\alpha_1 = \alpha_2 = \frac{100}{101}$

$V_{BB1} = V^+ \dfrac{R_2}{R_1 + R_2} \qquad R_{BB1} = R_1 \| R_2$

$V_{EE1} = -I_{B2} R_4 = -\dfrac{I_{C2}}{\beta} R_4 \qquad R_{EE1} = R_4$

$V_{BB2} = I_{E1} R_4 = \dfrac{I_{C1}}{\alpha} R_4 \qquad R_{BB2} = R_4$

Thus the two bias equations are

$$V^+ \frac{R_2}{R_1+R_2} + \frac{I_{C2}}{\beta} R_4 = \frac{I_{C1}}{\beta} R_1 \| R_2 + V_{BE} + \frac{I_{C1}}{\alpha} R_4$$

$$\frac{I_{C1}}{\alpha} R_4 = \frac{I_{C2}}{\beta} R_4 + V_{BE} + \frac{I_{C2}}{\alpha} R_6$$

It is left as a homework exercise to solve these simultaneously to obtain

$$I_{C1} = 1.41 \text{ mA} \qquad I_{C2} = 1.74 \text{ mA}$$

It is also left as an exercise to verify that $V_{CB} > 0$ for both transistors.