The MOSFET

Enhancement Device

\[ I_D = \frac{\mu C_{ox} W}{L} \left( 1 + \lambda V_{DS} \right) (V_{GS} - V_{TO})^2 \]

\( \mu \) = majority carrier mobility

\( C_{ox} \) = gate oxide capacitance per unit area

\( W \) = channel width

\( L \) = channel length

Depletion Device

For either device, the drain current is given by
\[ \lambda \text{ = channel length modulation parameter (reciprocal of the Early voltage)} \]

\[ V_{To} = \text{threshold voltage} \]

It is common to define \( K' \) as

\[ K' = \mu_C \text{Cox} \]

so that \( \lambda_D \) can be written

\[ \lambda_D = \frac{K'}{2} \frac{W}{L} (1 + \lambda V_{DS}) (V_{GS} - V_{To})^2 \]

This equation assumes the active or saturation mode. For the device to be in this mode, we must have

\[ V_{DS} > V_{GS} - V_{To} \]
For the enhancement mode device \( V_{To} > 0 \), for the depletion mode device \( V_{To} < 0 \).

To simplify the equation for \( i_D \), let us define

\[
K_0 = \frac{K'}{2} \frac{W}{L}
\]

\[
K = K_0 \left( 1 + 
\right)
\]

\[
\Rightarrow \quad i_D = K \left( V_{GS} - V_{TO} \right)^2
\]

Because the gate is insulated, \( i_G = 0 \). Thus \( i_S = i_D \).

The MOSFET Transfer Characteristics

The transfer characteristics are plots of \( i_D \) versus \( V_{GS} \) for \( V_{DS} = \text{constant} \). Let us assume an enhancement mode device
for which $V_{TO} > 0$.

\[ m = \text{slope} = \frac{\Delta I_D}{\Delta V_{GS}} \]

Draw a tangent line at the point $(V_{GS}, I_D)$. The slope of the line can be used to relate changes in $I_D$ to changes in $V_{GS}$.

\[ m = \frac{\Delta I_D}{\Delta V_{GS}} = 2K (V_{GS} - V_{TO}) \]

\[ = 2K \sqrt{\frac{I_D}{K}} \]

\[ = 2 \sqrt{K I_D} \]

\[ \Rightarrow \Delta I_D = 2 \sqrt{K I_D} \Delta V_{GS} \]
The MOSFET Output Characteristics

The output characteristics are plots of $i_D$ versus $V_{DS}$ for $V_{GS}$ = constant.

$$i_D = k_0 (1 + \lambda V_{DS}) (V_{GS} - V_{TO})^2$$

Draw a tangent line at the point $(V_{DS}, i_D)$. The slope of the line can be used to relate changes in $i_D$ to changes in $V_{DS}$.

$$m = \frac{di_D}{dV_{DS}} = k_0 \lambda (V_{GS} - V_{TO})^2$$
\[
\lambda \frac{I_D}{1 + \lambda V_{DS}} = \frac{I_D}{\frac{1}{\lambda} + V_{DS}}
\]

\[\Rightarrow I_d = \frac{I_D}{\frac{1}{\lambda} + V_{DS}} \cdot V_{ds} \]

Thus, in general, we have

\[I_d = 2\sqrt{K I_D} \cdot V_{gs} + \frac{I_D}{\frac{1}{\lambda} + V_{DS}} \cdot V_{ds} \]

Let us define

\[g_m = 2\sqrt{K I_D} \quad R_0 = \frac{\frac{1}{\lambda} + V_{DS}}{I_D} \]

\[\Rightarrow I_d = g_m V_{gs} + \frac{V_{gs}}{R_0} \]

Because the gate is insulated, it follows that

\[i_g = 0 \quad i_d = i_g + i_d = i_d \]
The Hybrid-π Model

The basic equations are

\[ i_d = g_m v_{gs} + \frac{v_{ds}}{n_0} \quad i_g = 0 \]

We can draw the model as follows:

The T Model

The T model puts a resistor in series with the i_d branch which has the same voltage across it as \( v_{gs} \) in the hybrid-π model.
We can write

\[ i'_d = i'_h = g_m \cdot v_{gh} \]

\[ \Rightarrow v_{gh} = \frac{i'_h}{g_m} \]

Let us define the resistance

\[ R_A = \frac{1}{g_m} \]

\[ \Rightarrow v_{gh} = i'_h \cdot R_A \]

Thus the T model is

\[ i'_d = i'_h = \frac{v_{gh}}{R_A} = g_m \cdot v_{gh} \]

Thus \( i'_d \) and \( i'_h \) are the same
as for the hybrid-π model. Also
\[ i_g = i_d - i_d = 0 \] which is the
same as for the hybrid-π
model.

**BJT/MOSFET Comparison**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>BJT</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( r_x )</td>
<td>&gt; 0</td>
<td>0</td>
</tr>
<tr>
<td>( g_m )</td>
<td>( I_c/V_T )</td>
<td>( 2/\sqrt{K I_D} )</td>
</tr>
<tr>
<td>( R_T )</td>
<td>( V_T/I_B )</td>
<td>( \infty )</td>
</tr>
<tr>
<td>( R_o )</td>
<td>( (V_A + V_CE)/I_c )</td>
<td>( 1 + V_{DS}/I_D )</td>
</tr>
<tr>
<td>( \beta )</td>
<td>( I_c/I_B )</td>
<td>( \infty )</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>( I_c/I_E )</td>
<td>1</td>
</tr>
<tr>
<td>( R_e = V_T/I_E )</td>
<td>( R_a = 1/g_m )</td>
<td></td>
</tr>
</tbody>
</table>

**The BJT Bias Equation**

Replace the dc circuits looking
out of the collector, base, and
emitter leads with Thévenin
equivalents.
The loop equation between the $V_{BB}$ and $V_{EE}$ nodes is

$$V_{BB} - V_{EE} = I_B R_{BB} + V_{BE} + I_E R_{EE}$$

Suppose we desire $I_C$. We use

$$I_B = \frac{I_C}{\beta} \quad I_E = \frac{I_C}{\alpha}$$

$$\Rightarrow V_{BB} - V_{EE} = I_C \frac{R_{BB}}{\beta} + V_{BE} + I_C \frac{R_{EE}}{\alpha}$$

$$\Rightarrow I_C = \frac{V_{BB} - V_{EE} - V_{BE}}{\frac{R_{BB}}{\beta} + \frac{R_{EE}}{\alpha}}$$
In a similar way, we obtain for \( I_E \)

\[
I_E = \frac{V_{BB} - V_{EE} - V_{BE}}{\frac{R_{BB}}{1+\beta} + R_{EE}}
\]

Example 1

![Circuit Diagram]

\( R_1 = 100 \, \text{k}\Omega \)
\( R_2 = 126 \, \text{k}\Omega \)
\( R_E = 5.6 \, \text{k}\Omega \)
\( \beta = 99 \)
\( \alpha = \frac{\beta}{1+\beta} = 0.99 \)
\( V_{BE} = 0.65 \, \text{V} \)

Solve for \( I_E \)

\[
V_{BB} = V^+ - \frac{R_2}{R_1 + R_2} + V^- - \frac{R_1}{R_1 + R_2} = 1.3636 \, \text{V}
\]

\[
R_{BB} = R_1 || R_2 = 54.45 \, \text{k}\Omega
\]
The equivalent circuit is

\[ V_{BB} - V^- = \frac{I_E}{1+\beta} \left( R_{BB} + V_{BE} + I_E R_E \right) \]

\[ \Rightarrow I_E = \frac{V_{BB} - V^- - V_{BE}}{\frac{R_{BB}}{1+\beta} + R_E} = 2.557 \text{ mA} \]

Our solution assumes the active mode. This requires \( V_{CB} > 0 \).

\[ V_C = V^+ - \alpha I_E R_C = 4.1151 \text{ V} \]

\[ V_B = V_E + V_{BE} = V^- + I_E R_E + V_{BE} = -0.0311 \text{ V} \]
\[ \Rightarrow V_{CB} = V_C - V_B = 4.1461 \, V \]

Because \( V_{CB} > 0 \), the BJT is in the active mode.

**Example 2**

\[ V^+ = 15 \, V \]

\[ R_1 = 20 \, k\Omega, \ R_2 = 10 \, k\Omega, \ R_3 = R_4 = 3 \, k\Omega, \ R_5 = R_6 = 2 \, k\Omega, \ V_{BE1} = V_{BE2} = 0.65 \, V \]

\[ \beta_1 = \beta_2 = 100, \ \alpha_1 = \alpha_2 = \frac{100}{101} \]

\[ V_{BB1} = V^+ \frac{R_2}{R_1 + R_2}, \quad R_{BB1} = R_1 \parallel R_2 \]

\[ V_{EE1} = -I_{B2} \frac{R_4}{\beta}, \quad R_{EE1} = R_4 \]

\[ V_{BB2} = I_{E1} \frac{R_4}{\alpha}, \quad R_{BB2} = R_4 \]
Thus the two bias equations are

\[ V^+ \frac{R_2}{R_1+R_2} + \frac{Ic_2}{\beta} R_4 = \frac{Ic_1}{\beta} R_{11} R_2 + V_{BE} + \frac{Ic_1}{\alpha} R_4 \]

\[ \frac{Ic_1}{\alpha} R_4 = \frac{Ic_2}{\beta} R_4 + V_{BE} + \frac{Ic_2}{\alpha} R_6 \]

It is left as a homework exercise to solve these simultaneously to obtain

\[ Ic_1 = 1.41 \text{ mA} \quad Ic_2 = 1.74 \text{ mA} \]

It is also left as an exercise to verify that \( V_{CB} > 0 \) for both transistors.