7. DESIGN PROJECT—FALL 2006

7.1 Objective

The objective of this experiment is to design, simulate, evaluate experimentally, and document a low-noise feedback amplifier circuit. The equivalent input noise of the amplifier is to be minimized.

7.2 Specifications

The topology used for the feedback amplifier is two internal stages of voltage gain. The first stage is to be discrete. The second stage may be either discrete or an op amp.

The specifications for the feedback amplifier are:

- DC Power Supplies: either $\pm 15\,\mathrm{V}$
- Closed Loop Voltage Gain: $30\,\mathrm{dB}$
- Maximum Input Signal $200\,\mathrm{mV}$
- Lower Half-Power Frequency: $20\,\mathrm{Hz}$ or less
- Upper Half-Power Frequency: $20\,\mathrm{kHz}$ or greater
- THD (total harmonic distortion): less than 0.4% corresponding to an output signal level of $+10\,\mathrm{dBm}$ for an input sine wave with a frequency of $2\,\mathrm{kHz}$
- Source Resistance: $10\,\mathrm{k}\Omega$
- Load Resistance: $600\,\Omega$
- Noise voltage over the band $20\,\mathrm{Hz}$ to $20\,\mathrm{kHz} \leq 1\,\mu\mathrm{V}$.

7.3 Simulation

The initial design should be verified with a SPICE simulation. This simulation must precede the circuit assembly.

Should the designer elect to employ a BJT as the first stage, the default values for `IS`, `BF`, `RB`, `VA`, `CJC`, `CJE`, and `TF` for the BJT transistor are not to be used for the simulation. Instead, use the values obtained from curve tracer measurements or manufacturers' data sheets. The value of the base spreading resistance measured in a previous experiment is to be used as `RB`. (In determining the optimum collector current use an average or typical value that was measured for the transistor.)

A noise simulation of the circuit should be made which predicts the signal-to-noise ratio corresponding to an output signal level of +10 dBm into 600 Ω and noise figure of the amplifier.

The SPICE analyses should include `.OP` (to verify the biasing), `.AC` (to verify the frequency response specifications and phase margin specifications), `.TRAN` (to examine the clipping and slew rate performance), `.FOUR` (to verify the distortion specification), and `.NOISE` (to verify the noise specifications).

7.4 Experimental Measurements

Assemble the designed circuit on a solderless breadboard with a 600 Ω load resistor. Use a power supply decoupling network.

Use the laboratory equipment to measure and record the circuit:

- mid-band voltage gain
- − 3 dB bandwidth
- positive and negative slew rates
- distortion @ $f = 2$ kHz
- quiescent operating point
- output DC offset with input grounded
- equivalent input noise voltage
- signal-to-noise ratio
- noise figure (spot noise figure @ $f = 2$ kHz and the total noise figure)

The noise measurements are made with the source grounded. The other measurements are made with the function generator as the source.

7.5 Laboratory Report

The laboratory report should simply, succinctly, and lucidly summarize the design philosophy, present the appropriate calculations, and compare the theoretical, simulation, and experimental results.

The design project will weighted as three lab reports and will graded somewhat more critically than the previous reports. Although the design project grade will in part depend on the write-up, the major criterion will be whether or not the circuit meets the design criteria.

7.6 Due Date

Friday, December 1, 2006 A. D.