Chapter 5

JFET Noise

Object

The objects of this experiment are to measure the spectral density of the noise current output of a JFET, to compare the measured density to the theoretical density, and to determine the lower corner frequency below which excess noise generated by generation-recombination centers in the intrinsic region of the JFET dominates.
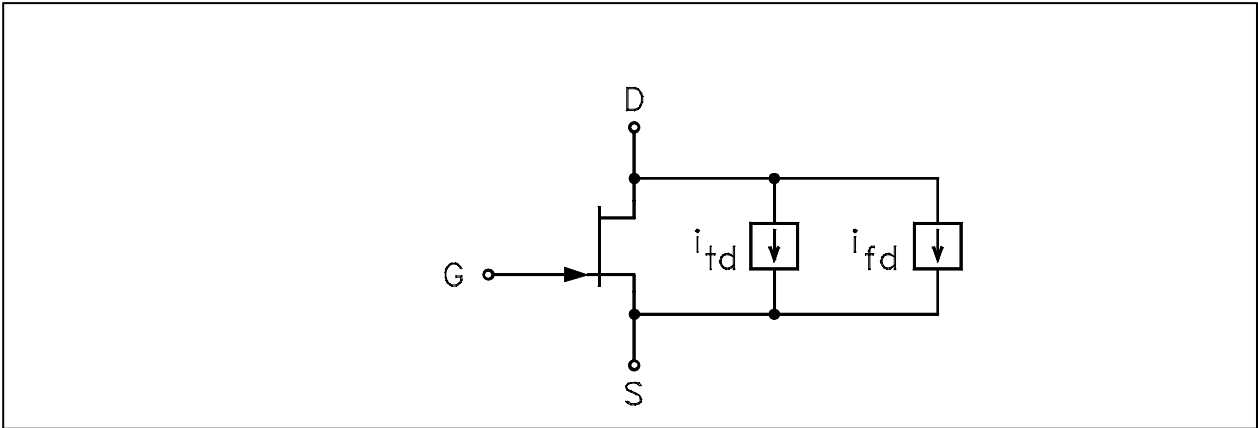
Theory

Figure 5.1: JFET noise equivalent circuit.

The noise equivalent circuit of a JFET is given in Fig. 5.1 where i_{td}^2 is the mean-square thermal drain noise current and i_{fd}^2 is the excess or mean-square flicker noise current. These are given by

$$i_{td}^2 = 4kT \left(\frac{2g_m}{3} \right) \Delta f \tag{5.1}$$

$$i_{fd}^2 = \frac{K_f I_D}{f} \Delta f \tag{5.2}$$

where g_m is the small-signal JFET transconductance and K_f is the flicker noise coefficient. The small-signal transconductance of the JFET is related to its pinchoff voltage V_P and its drain-to-source saturation current I_{DSS} by

$$g_m = \frac{-2}{V_P}\sqrt{I_D I_{DSS}} \tag{5.3}$$

where I_D is the quiescent drain current. This current is related to the quiescent gate-to-source voltage by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \tag{5.4}$$

where it is assumed that the JFET is operated in its saturation region and that the drain current is not a function of the drain-to-source voltage in this region. It should be borne in mind that both the gate-to-source voltage and the pinch off voltage are negative for an N channel JFET. This makes the small signal transconductance g_m positive.

The relationship between the drain current and gate-to-source voltage may also be expressed using as alternative set of parameters known as the threshold voltage V_{TO} and transconductance parameter β for the JFET. These are the JFET parameters used with SPICE. (One should not confuse this beta with the one used as the current gain for a BJT.) These parameters are related to the drain-to-source saturation current and pinch off voltage by

$$V_{TO} = V_P \tag{5.5}$$

and

$$\beta = \frac{I_{DSS}}{V_P^2} \tag{5.6}$$

which means that

$$I_D = \beta\left(V_{GS} - V_{TO}\right)^2 \tag{5.7}$$

and

$$g_m = 2\sqrt{\beta I_D} \tag{5.8}$$

The flicker noise coefficient is given by

$$K_f = \frac{16kT}{3}f_L\sqrt{\frac{\beta}{I_D}} \tag{5.9}$$

which means that the mean-squared flicker noise current can also be expressed as

$$i_{fd}^2 = 4kT\left(\frac{2g_m}{3}\right)\frac{f_L}{f}\Delta f \tag{5.10}$$

This illustrates that the corner frequency f_L is the frequency at which the mean squared thermal and flicker currents are equal in magnitude. Thus the corner frequency may be experimentally determined by measuring the frequency at which the total noise current increases by $3\,\mathrm{dB}$ over the value in the region at which thermal noise dominates where the response is flat or white.

Laboratory Procedure

Curve Tracer Measurements

The power supply voltages for this circuit are V^+ and V^-, the positive and negative power supply voltages respectively. For symmetry's sake these will be selected as $|V^+| = |V^-|$. Either $\pm 15\,\text{V}$ may be chosen if the circuit is assembled using the laboratory bench dc power supply or $\pm 9\,\text{V}$ if batteries are employed.

Use the transistor curve tracer to measure the I_D of the JFET at a gate-to-source voltage of $0\,\text{V}$ and a drain-to-source voltage of $V^+/2$. If the JFET is pinched off, this drain current will be I_{DSS}. Next, use the input generator on the curve tracer to reverse bias the gate-to-source junction until the drain current has been reduced to $I_{DSS}/2$. Record the value of the gate-to-source voltage (remember that both the gate-to-source voltage and the pinchoff voltage are negative for an N channel JFET). From the data obtained, calculate the pinch off voltage of the JFET and its transconductance at a quiescent drain current of $I_{DSS}/2$.
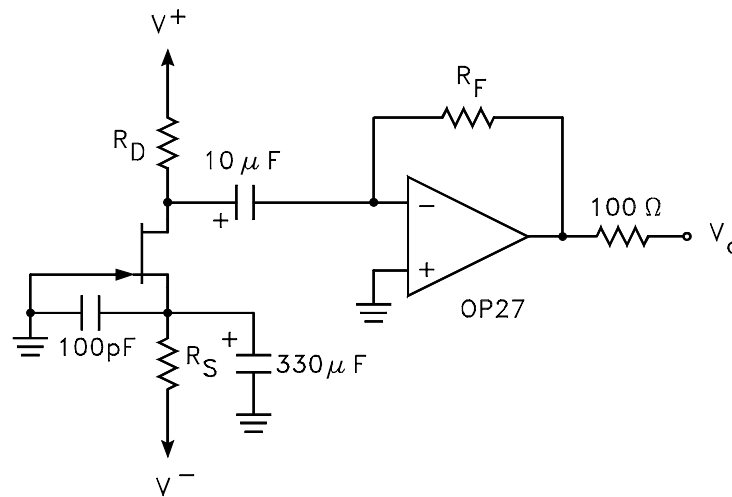

Figure 5.2: JFET noise measurement.

Biasing

The circuit shown in Fig. 5.2 is the test circuit for measuring the noise produced by the JFET. When this circuit is assembled on the solderless breadboard, the power supply rails should be decoupled with a $100\,\Omega$ resistor and a $100\,\mu\text{F}$ capacitor. If available, use batteries as the power supply and use the shielded boxes to enclose the breadboard. The JFET is to be operated at a drain-to-source voltage of $V^+/2$ and a drain current of $I_{DSS}/2$ as determined in the previous step. For this current, the correct value of R_S is given by

$$R_S = \frac{-V^- - V_{GS}}{I_D} \tag{5.11}$$

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where V_{GS} is the gate-to-source voltage determined in the previous step at which $I_D = I_{DSS}/2$. (Remember that both V^- is negative and V_{GS} is also negative for an N channel JFET.) To bias the drain-to-source voltage at $V^+/2$, the correct value of R_D is given by

$$R_D = \frac{V^+/2 + V_{GS}}{I_D} \tag{5.12}$$

With the calculated values of R_S and R_D, assemble the circuit on the breadboard and verify that the bias current and voltages are correct, i.e. that they are within 5% of the design values. The choice of R_F is somewhat arbitrary. The larger R_F is the larger the voltage at the output will be. Initially, select $R_F = 100\,\text{k}\Omega$.

Frequency Response

Experimentally determine the frequency response of the JFET and the bifet-op-amp combination. Disconnect the short from the gate to ground, place a resistor $(11\,\text{k}\Omega)$ from the gate to ground and place a large coupling capacitor (e.g. $10\,\mu\text{F}$) between the gate and the function generator output. The theoretical value of the voltage gain is

$$A_v = \frac{V_o}{V_g} = g_m R_F \tag{5.13}$$

where V_g is the voltage at the output of the function generator.

Assemble the circuit again as shown in Fig. 5.2. Namely, remove the function generator, coupling capacitor, and resistors from the gate to the positive and negative power supplies. Connect a short from the gate to ground.

Background Noise, JFET Noise, and Corner Frequency

After it has been verified that the circuit is functioning properly, remove the JFET from the circuit and connect the Dynamic Signal Analyzer to the output of the op amp. Using a total analysis band of $100\,\text{kHz}$, measure the spectra of the background noise generated by R_D and the op-amp circuit. After doing this, reconnect the JFET to the circuit and remeasure the spectra of the noise. (For accuracy in the calculations, the noise with the JFET should be several dB higher than the noise without the JFET. If it isn't a larger value of R_F may be used.) From the spectra observed, decide on an optimum frequency to measure the noise so that the midband white noise generated by the JFET is not corrupted with the excess or flicker noise. Plot the spectra obtained. From the display, determine the corner frequency, f_L, which will be the frequency at which the output voltage of the op amp increases by $3\,\text{dB}$ from the value in the flat region.

Laboratory Report

Formula Verification

Verify the formulas for g_m, R_S, and R_D that were given in the theory and procedures sections.

Comparison of Experimental and Theoretical Spectra

Compare the measured noise spectral density for the white noise region of the spectrum to that predicted by the theoretical formula for i_{td}^2. What is the lower corner frequency below which the excess noise dominates? A major source of error in this calculation will be the excess noise in the measurement system. If this dominates, the excess noise generated by the JFET may be difficult to determine.

Computation of v_n^2

Reflect i_{td}^2 and i_{fd}^2 noise sources to the gate of the JFET and compute the v_n^2 for this transistor. Use the experimental data from 5 of the procedure. (Divide the voltage at the output of the op amp by $g_m R_F$.)

Due Date

The written laboratory report is due one week from the date the experiment was performed unless otherwise stated.