Can "Transconductance Doubling" Occur with Class-AB Output Stages?

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It is said by some that the transconductance of a class-AB output stage increases when the output voltage passes through the crossover region where both transistors are conducting. Outside the crossover region, only one transistor conducts. Thus it is said that the transconductance decreases. To investigate this for a BJT complementary common-collector output stage, consider the circuit shown in Fig. 1. A two-transistor BJT output stage is shown with two bias sources labeled V_B which set the quiescent current in the transistors. The emitter currents can be written

$$i_{E1} = I_S \left[\exp\left(\frac{v_I + V_B - v_O}{V_T} \right) - 1 \right] \tag{1}$$

$$i_{E2} = I_S \left[\exp\left(\frac{v_O + V_B - v_I}{V_T} \right) - 1 \right] \tag{2}$$

where I_S is the saturation current, $\exp(x)$ is the exponential function, and V_T is the thermal voltage. The output current is given by

$$\begin{aligned} i_O &= i_{E1} - i_{E2} \\ &= I_S \left[\exp\left(\frac{v_I + V_B - v_O}{V_T} \right) - \exp\left(\frac{v_O + V_B - v_I}{V_T} \right) \right] \\ &= 2I_S \exp\left(\frac{V_B}{V_T} \right) \sinh\left(\frac{v_I - v_O}{V_T} \right) \end{aligned} \tag{3}$$

where $\sinh(x)$ is the hyperbolic sine function.

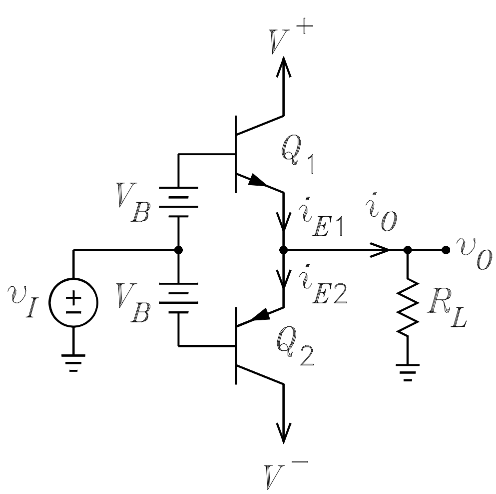

Figure 1: Class-AB output stage.

When $v_I = 0$, it follows that $v_O = 0$ and $i_O = 0$. In this case, the emitter currents are equal to the quiescent bias current I_B given by

$$I_B = I_S \left[\exp\left(\frac{V_B}{V_T} \right) - 1 \right] \tag{4}$$

It follows from this equation that i_O can be written

$$i_O = 2\left(I_B + I_S\right) \sinh\left(\frac{v_I - v_O}{V_T} \right) \tag{5}$$

Thus the output voltage is given by

$$v_O = i_O R_L = 2\left(I_B + I_S\right) R_L \sinh\left(\frac{v_I - v_O}{V_T} \right) \tag{6}$$

The small-signal transconductance of the output stage is given by

$$g_m = \frac{di_O}{dv_I} \tag{7}$$

By implicit differentiation of Eq. (5), we have

$$g_m = 2\left(I_B + I_S\right) \cosh\left(\frac{v_I - v_O}{V_T} \right) \times \frac{1}{V_T} \left(1 - \frac{dv_O}{dv_I} \right) \tag{8}$$

where $\cosh(x)$ is the hyperbolic cosine function. But dv_O/dv_I can be written

$$\frac{dv_O}{dv_I} = \frac{di_O}{dv_I} \times \frac{dv_O}{di_O} = g_m R_L \tag{9}$$

Thus we have

$$g_m = 2\left(I_B + I_S\right) \cosh\left(\frac{v_I - v_O}{V_T} \right) \times \frac{1}{V_T} \left(1 - g_m R_L \right) \tag{10}$$

This can be solved for g_m to obtain

$$g_m = \left[R_L + \frac{V_T}{2\left(I_B + I_S\right)} \operatorname{sech}\left(\frac{v_I - v_O}{V_T} \right) \right]^{-1} \tag{11}$$

where $\operatorname{sech}(x)$ is the hyperbolic secant function. The small-signal voltage gain A_v is equal to $g_m R_L$ and is given by

$$A_v = g_m R_L = \left[1 + \frac{V_T}{2\left(I_B + I_S\right) R_L} \operatorname{sech}\left(\frac{v_I - v_O}{V_T} \right) \right]^{-1} \tag{12}$$

Because A_v represents the transconductance g_m multiplied by the constant R_L, it can be considered to be a normalized transconductance, i.e. it is normalized by the constant R_L. Eq. (6) can be used to express A_v as a function of v_O only to obtain

$$A_v = \left\{ 1 + \frac{V_T}{2\left(I_B + I_S\right) R_L} \operatorname{sech}\left[\sinh^{-1}\left(\frac{v_O}{2\left(I_B + I_S\right) R_L} \right) \right] \right\}^{-1} \tag{13}$$

With the use of the identity $\operatorname{sech}(x) = 1/\sqrt{1+\sinh^2(x)}$, this can be rewritten

$$A_v = \left[1 + \frac{\dfrac{V_T}{2\,(I_B + I_S)\,R_L}}{\sqrt{1 + \left[\dfrac{v_O}{2\,(I_B + I_S)\,R_L} \right]^2}} \right]^{-1} \tag{14}$$

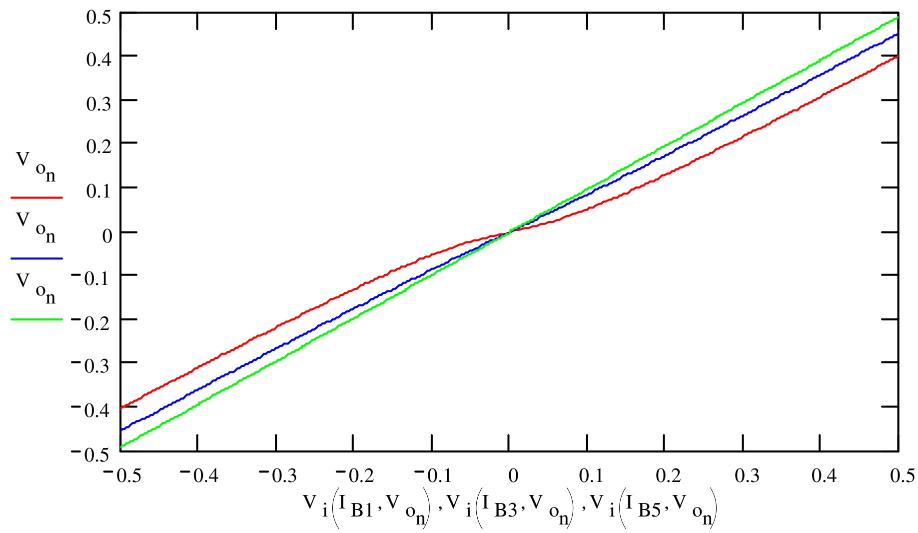

Figure 2: Plots of output voltage versus input voltage for three bias currents.

Figure 2 shows plots of the output voltage with an $8\,\Omega$ load for $I_B + I_S = 1\,\mathrm{mA}$, $9\,\mathrm{mA}$, and $81\,\mathrm{mA}$. Fig. 3 shows plots of the small-signal voltage gain A_v with an $8\,\Omega$ load for $I_B + I_S = 1\,\mathrm{mA}$, $3\,\mathrm{mA}$, $9\,\mathrm{mA}$, $27\,\mathrm{mA}$, and $81\,\mathrm{mA}$. The plots assume that $V_T = 25\,\mathrm{mV}$. For a typical BJT used in the output stage of an amplifier, the saturation current I_S has a value on the order of $10^{-12}\,\mathrm{A}$. Thus $I_B + I_S \simeq I_B$ for all of the curves. It can be seen from Fig. 3 that the small-signal voltage gain, i.e. the transconductance multiplied by the constant R_L, never exceeds unity in the crossover region for the assumed bias currents. If it did, the common-collector stage would exhibit a small-signal voltage gain greater than unity, which is impossible. Thus larger bias currents result in a small-signal voltage gain or normalized transconductance that is closer to unity, but never greater than unity, in the crossover region.

The curves in Figs. 2 and 3 are calculated assuming no resistors in series with the emitters of the transistors. This is because it is impossible to solve the nonlinear BJT equations for the transconductance of the stage if these resistors are in the circuit. In practice, series emitter resistors in the range $0.1\,\Omega \le R_E \le 0.33\,\Omega$ are used to stabilize the bias currents in the transistors and as current sense resistors in protection circuits. The addition of these resistors causes the transconductance to decrease for all values of output current. However, the transconductance decreases less in the crossover region than well away from the crossover region. In the crossover region, the transconductance is reduced from the value

$$g_m = \frac{2I_B}{V_T} \tag{15}$$

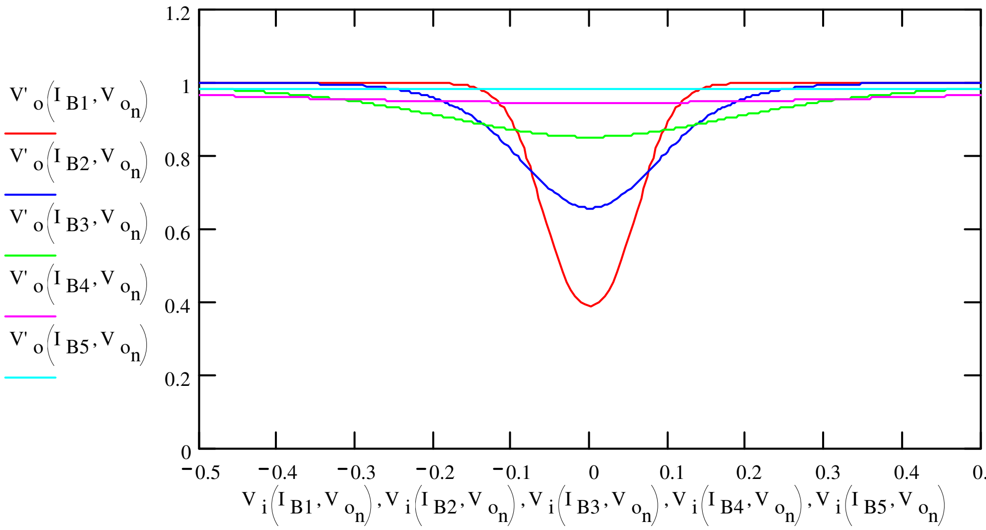

Figure 3: Plots of small-signal voltage gain, i.e. normalized transconductance, for eight bias currents.

to the value

$$g_m = \frac{2I_B}{V_T + I_B R_E} \tag{16}$$

Well away from the crossover region the transconductance is reduced from the value

$$g_m = \frac{|i_O|}{V_T} \tag{17}$$

to the value

$$g_m = \frac{|i_O|}{V_T + |i_O| R_E} \tag{18}$$

For $|i_O|$ large, this approaches

$$g_m = \frac{1}{R_E} \tag{19}$$

For the transconductance in the crossover region to equal the transconductance well away from the crossover region, it follows that the equation

$$\frac{2I_B}{V_T} = \frac{2I_B}{V_T + I_B R_E} \tag{20}$$

must hold. Solution of this equation for R_E yields

$$R_E = \frac{V_T}{I_B} \tag{21}$$

Any value of R_E greater than the value given by this equation causes the transconductance in the crossover region to exceed the transconductance well away from the crossover region. To calculate a typical value predicted by the equation, let $V_T = 25\,\text{mV}$ and $I_B = 25\,\text{mA}$.

We obtain $R_E = 1\,\Omega$. This is much larger than the value typically used for R_E. Thus we could conclude that transconductance doubling cannot be caused by the addition of emitter resistors with values that are typically used in output stages.

Figure 4 shows example SPICE plots of the variation of the transconductance with output voltage for the BJT stage with and without emitter resistors. The upper curve is for $R_E = 0$. The lower curve is for $R_E = 0.22\,\Omega$. In each case, the bias current in each transistor is $I_B = 100\,\mathrm{mA}$ and the load resistance is $R_L = 8\,\Omega$. Note that the scale is very expanded, showing the transconductance over the range from 120 mS to 125 mS. Without the emitter resistors, the transconductance exhibits a dip of 1.36% in the crossover region. With the emitter resistors, the transconductance exhibits an equal ripple characteristic with two dips of 0.504% on each side of 0 V. The total deviation with the emitter resistors has been reduced by a factor of 2.69. Thus the transconductance is almost three times more linear with the emitter resistors than without them. However, the transconductance is lower for all values of output currrent.

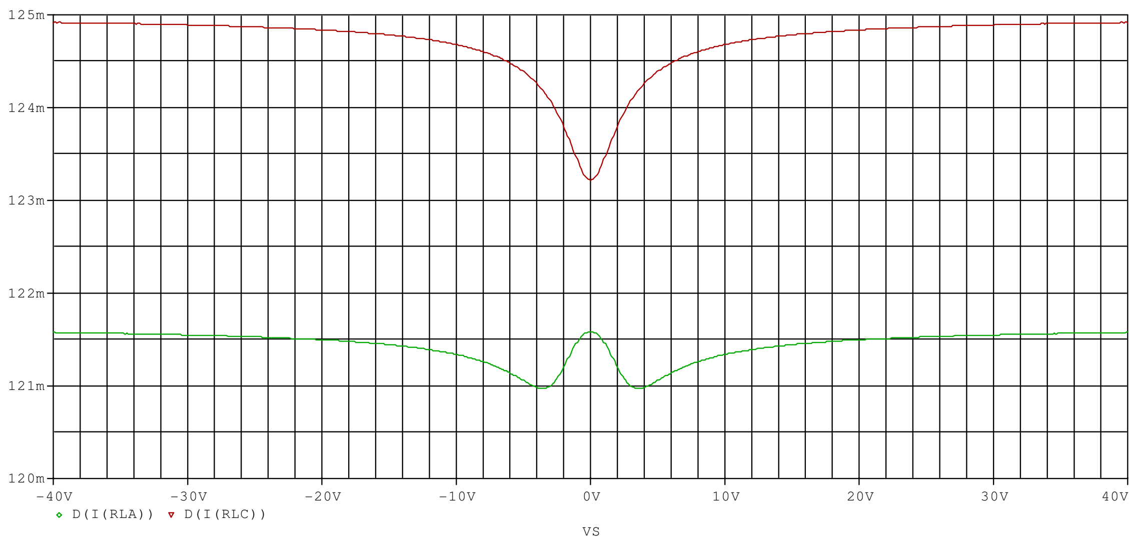

Figure 4: Transconductance plots versus output voltage. Upper curve without emitter resistors. Lower curve with emitter resistors.

Figure 5 shows a complementary common-drain MOSFET output stage. The source currents can be written

$$i_{S1} = K\left(v_I + V_B - v_O - V_{TO}\right)^2 \times u\left(v_I + V_B - v_O - V_{TO}\right) \tag{22}$$

$$i_{S2} = K\left(v_O + V_B - v_I - V_{TO}\right)^2 \times u\left(v_O + V_B - v_I - V_{TO}\right) \tag{23}$$

where K is the transconductance parameter, V_{TO} is the threshold voltage, and $u(x)$ is the unit step function given by

$$\begin{aligned} u(x) &= 0 \text{ for } x < 0 \\ &= 1 \text{ for } x \geq 0 \end{aligned} \tag{24}$$

The output current and voltage are given by

$$i_O = i_{S1} - i_{S2} \tag{25}$$

$$v_O = i_O R_L = (i_{S1} - i_{S2})\, R_L \tag{26}$$

When $v_I = 0$, it follows that $v_O = 0$. In this case, the two source currents are equal to the quiescent bias current I_B given by

$$I_B = K\,(V_B - V_{TO})^2 \tag{27}$$

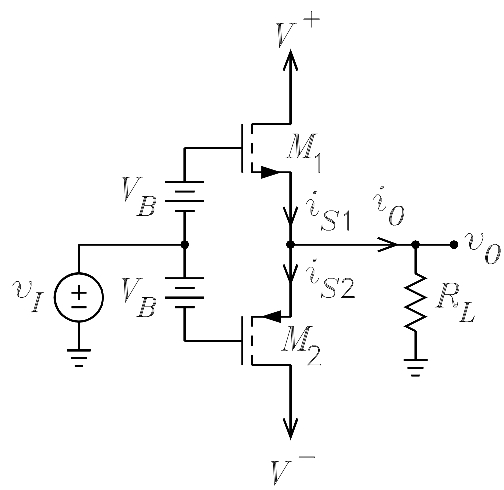

Figure 5: Class-AB complementary common-drain output stage.

Equations (22), (23), (26) and (27) can be solved simultaneously to obtain the equation

$$\begin{aligned} v_I \;=\;& \left[v_O - \frac{1}{\sqrt{K}}\left(\sqrt{\frac{-v_O}{R_L}} - \sqrt{I_B}\right)\right] \times u\,(-v_O - 4I_B R_L) \\ &+ \left(1 + \frac{1}{4R_L\sqrt{KI_B}}\right) v_O \times \left[u\,(v_O + 4I_B R_L) - u\,(v_O - 4I_B R_L)\right] \\ &+ \left[v_O + \frac{1}{\sqrt{K}}\left(\sqrt{\frac{v_O}{R_L}} - \sqrt{I_B}\right)\right] \times u\,(v_O - 4I_B R_L) \end{aligned} \tag{28}$$

The small-signal voltage gain can be obtained by implicit differentiation of Eq. (28) to obtain

$$\begin{aligned} \frac{v_o}{v_i} \;=\;& \frac{dv_O}{dv_I} \\ =\;& \frac{\sqrt{-4KR_Lv_O}}{1 + \sqrt{-4KR_Lv_O}} \times u\,(-v_O - 4I_B R_L) \\ &+ \frac{4R_L\sqrt{KI_B}}{1 + 4R_L\sqrt{KI_B}} \times \left[u\,(v_O + 4I_B R_L) - u\,(v_O - 4I_B R_L)\right] \\ &+ \frac{\sqrt{4KR_Lv_O}}{1 + \sqrt{4KR_Lv_O}} \times u\,(v_O - 4I_B R_L) \end{aligned} \tag{29}$$

Because $v_o/v_i = g_m R_L$, this equation represents the transconductance g_m multiplied by the constant R_L, i.e. the normalized transconductance.

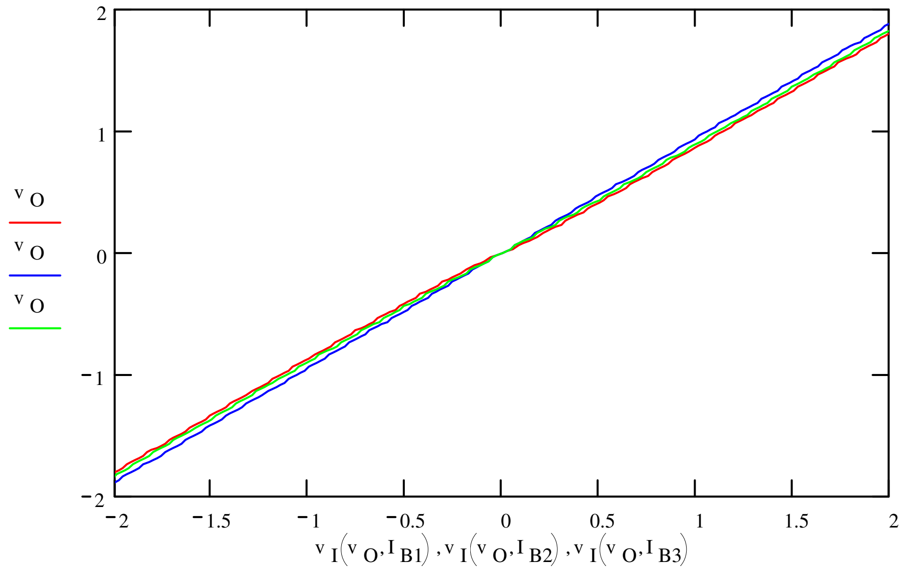

Figure 6: Plots of output voltage versus input voltage for three bias currents.

Figures 6 and 7 show plots of the output voltage versus input voltage and the small-signal voltage gain, i.e. the normalized transconductance, versus input voltage for the load resistance $R_L = 8\,\Omega$ and the bias currents $I_B = 1\,\mathrm{mA}$, $10\,\mathrm{mA}$, and $50\,\mathrm{mA}$. The MOSFET transconductance parameter used for the calculations is $K = 5$. It can be seen from Fig. 7 that the transconductance in the central class-A region where both transistors are conducting is a constant. Outside this region, the transconductance increases as $|v_I|$ increases. Increasing the bias current I_B cannot cause the transconductance in the class-A region to be greater than its value in the class-B regions. Because the transconductance of the MOSFET us usually lower than it is for a BJT, the addition of resistors in series with the sources of the MOSFETs would have less effect on the transconductance than with the BJT circuit.

To see how the fallacy of "transconductance doubling" has arisen, consider the complementary common-collector amplifier shown in Fig. 8. The dc bias current in the two transistors is set by the dc sources labeled V_B. The output current is given by $i_O = i_{E1} - i_{E2}$. Let the transistors have the typical SPICE parameters $\beta = 100$ and $I_S = 4.448\,\mathrm{pA}$ and the circuit element values $V^+ = 50\,\mathrm{V}$, $V^- = -50\,\mathrm{V}$, $V_B = 0.65\,\mathrm{V}$, $R_E = 0.22\,\Omega$, and $R_L = 8\,\Omega$. With these values, the bias current in each transistor is $118\,\mathrm{mA}$.

Fig. 9 shows the SPICE simulation of i_O versus v_I. The upper curve labeled Q1 is i_{E1}, the lower curve labeled Q2 is $-i_{E2}$, and the center curve which passes through the origin is $i_O = i_{E1} - i_{E2}$. (By convention, SPICE assumes all transistor currents are positive when they flow into the device. Thus the -IE(Q1) labeled on the horizontal axis in the figure corresponds to i_{E1} in Fig. 8.) Note the very linear combined response in the center curve. At any point, the slope of this curve is the small-signal transconductance. For all practical purposes, it is a constant.

Now, let us simulate an incorrect version of the circuit which seems to be the source of the fallacy of "transconductance doubling." Let us assume that the emitter current in each transistor can be calculated independently of the other transistor and then the two currents

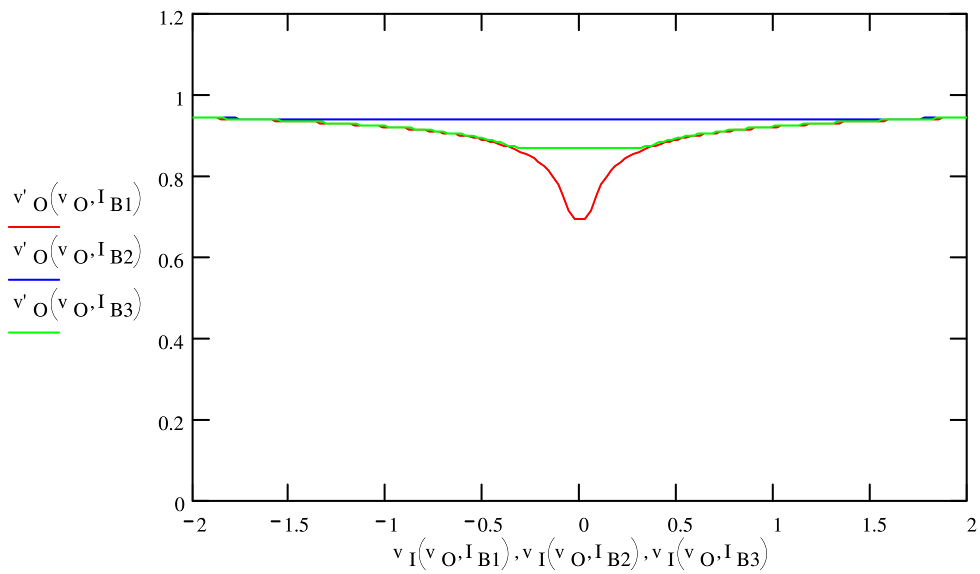

Figure 7: Plots of small-signal voltage gain, i.e. normalized transconductance, for three bias currents.

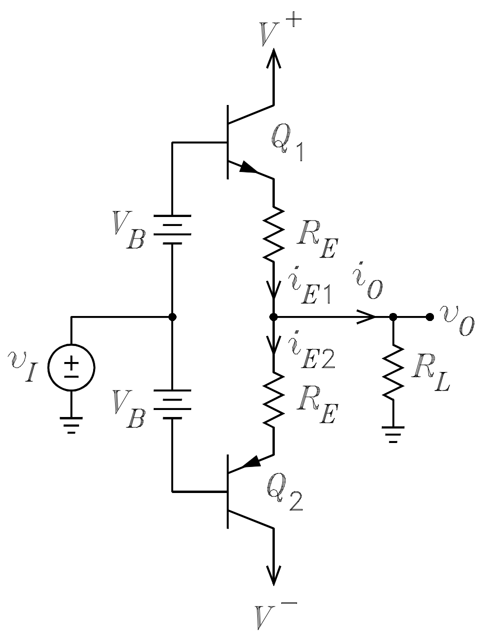

Figure 8: Class-AB output stage.

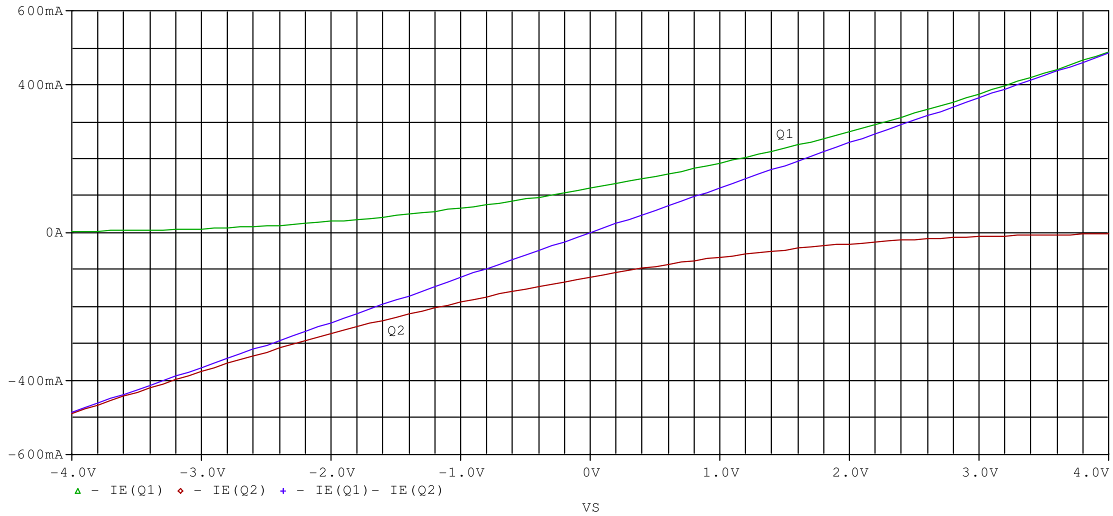

Figure 9: SPICE plots of i_{E1}, $-i_{E2}$, and $i_O = i_{E1} - i_{E2}$ versus v_I for the circuit in Fig. 8.

can be combined to obtain the output current. The modified circuit is shown in Fig. 10. This figure shows the original circuit with a separate load resistor on each transistor and the transistors disconnected from each other. In order for the dc bias currents to be the same, the value of V_B was changed to 1.596 V.

Fig. 11 shows the results of the SPICE simulation of the circuit in Fig. 10. The upper curve labeled Q1 is i_{E1}, the lower curve labeled Q2 is $-i_{E2}$, and the center curve which passes through the origin is $i_{E1} - i_{E2}$. For $-1\,\mathrm{V} < v_I < +1\,\mathrm{V}$, this figure shows the center curve exhibiting a doubling in its slope. Because the small-signal transconductance is the slope of the i_O versus v_I curve, it appears that the transconductance has doubled in the crossover region. But the currents in this figure are not correct. The correct currents are shown in Fig. 9, which shows no evidence of "transconductance doubling." For anyone who would like to experiment further with the SPICE simulations, the netlists are given below.

SPICE Netlist for the simulation of Fig. 9:

```
FIGURE 9 SIMULATION
VS 1 0 DC 0
VPLUS 4 0 DC 50
VMINUS 5 0 DC -50
VB1A 2 1 DC 0.65
VB2A 1 3 DC 0.65
Q1 4 2 6 NMOD
Q2 5 3 7 PMOD
RE1 6 8 0.22
RE2 7 8 7 0.22
RLA 8 0 8
.MODEL NMOD NPN IS=3.984E-12
.MODEL PMOD PNP IS=3.984E-12
.OP
```

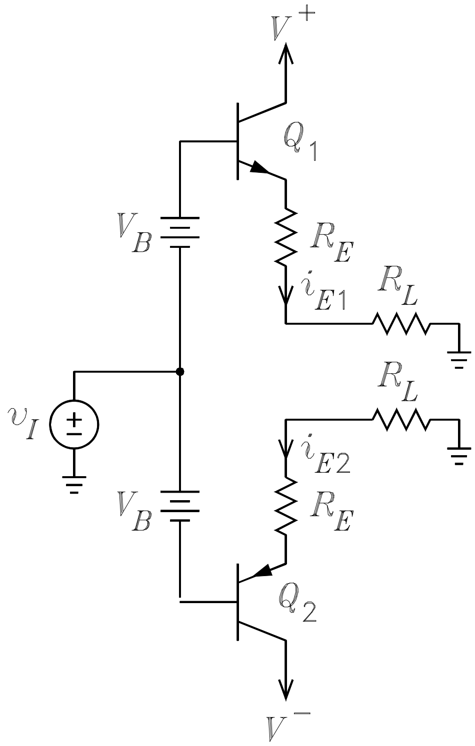

Figure 10: Class-AB stage with the emitters of the transistors disconnected.

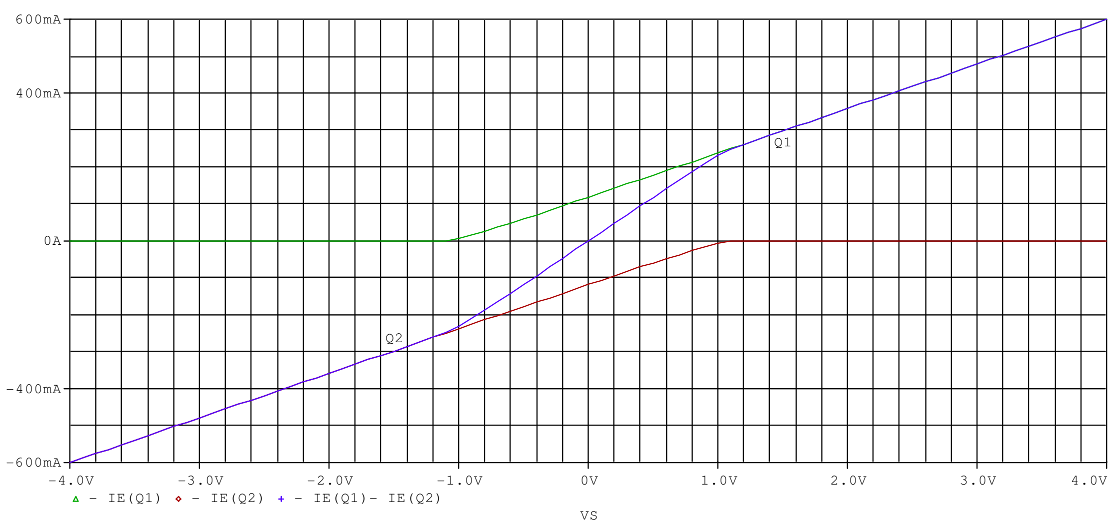

Figure 11: SPICE plots i_{E1}, $-i_{E2}$, and $i_{E1} - i_{E2}$ versus v_I for the circuit in Fig. 10.

```
.DC VS -4 4 0.1
.PROBE
.END
```

SPICE Netlist for the simulation of Fig. 11:

```
FIGURE 11 SIMULATION
VS 1 0 DC 0
VPLUS 4 0 DC 50
VMINUS 5 0 DC -50
VB1B 2 1 DC 1.596
VB2B 1 3 DC 1.596
Q1 4 2 6 NMOD
Q2 5 3 7 PMOD
RE1 6 8 0.22
RE2 7 9 0.22
RLA 8 0 8
RLB 9 0 8
.MODEL NMOD NPN IS=3.984E-12
.MODEL PMOD PNP IS=3.984E-12
.OP
.DC VS -4 4 0.1
.PROBE
.END
```