7. DESIGN PROJECT—FALL 2010

7.1 Objective

The objective of this experiment is to design, simulate, evaluate experimentally, and document a low-noise electronic amplifier circuit. The circuit is a published low-noise preamplifier design. The equivalent input noise of the amplifier is to be minimized, viz. the noise performance of the amplifier is to be optimized with respect to the output noise.

7.2 Specifications

The topology is contained in
http://sound.westhost.com/project66.htm

The power supply voltages are to be reduced from 15 to 9 V and the circuit is to be rebiased for optimal noise performance. The NPN transistor shown is not one stocked and a 2N4401 is to be used instead.

The specifications for the amplifier are:

- DC Power Supplies: ± 9 V
- Small-Signal Midband Voltage Gain: 60 dB
- Minimum Output Signal for which the THD is to be 0.2% or less $2\sqrt{2}$ V peak, viz. an rms value of 2 V. The THD is to be measured for a input which is a sine wave with a frequency of 2 kHz.The value of the input is that which makes the output 2 V rms.
- Lower Half-Power Frequency: 20 Hz or less
- Upper Half-Power Frequency: 20 kHz or greater
- Source Resistance: 200 Ω
- Load Resistance: 12 kΩ
- Noise voltage over the band 20 Hz to 20 kHz optimal, viz. lowest noise that can be obtained at the output port
- Devices. The devices are restricted to those available for this course, viz. Transistors: 2N4401 NPN BJT, 2N3904 NPN BJT, 2N4403 PNP BJT, 2N3906 PNP BJT, Op Amps 741, TL071

7.3 Simulation

The initial design should be verified with a SPICE simulation. This simulation must precede the circuit assembly.

The default values for `IS`, `BF`, `RB`, `VA`, `CJC`, `CJE`, and `TF` for the BJT transistor are not to be used for the simulation. Instead, use the values obtained from curve tracer measurements or manufacturers' data sheets. The value of the base spreading resistance measured in a previous experiment is to be used as `RB`. (In determining the optimum collector current use an average or typical value that was measured for the transistor.)

A noise simulation of the circuit should be made which predicts the signal-to-noise ratio corresponding to an output signal level of 2 V rms and noise figure of the amplifier.

The SPICE analyses should include `.OP` (to verify the biasing), `.AC` (to verify the frequency response specifications and phase margin specifications), `.TRAN` (to examine the clipping and slew rate performance), `.FOUR` (to verify the distortion specification), and `.NOISE` (to verify the noise specifications).

7.4 Experimental Measurements

Assemble the designed circuit on a solderless breadboard with a 12 kΩ load resistor. Use a power supply decoupling network.

Use the laboratory equipment to measure and record the circuit:

- mid-band voltage gain
- − 3 dB bandwidth
- positive and negative slew rates
- distortion @ $f = 2$ kHz and output signal 2 V rms
- quiescent operating point
- output DC offset with input grounded
- equivalent input noise voltage
- signal-to-noise ratio (where output signal is 2 V rms
- noise figure (spot noise figure @ $f = 2$ kHz and the total noise figure)

The noise measurements are made with the source grounded. The other measurements are made with the function generator or the signal analyzer as the source.

7.5 Laboratory Report

The laboratory report should simply, succinctly, and lucidly summarize the design philosophy, present the appropriate calculations, and compare the theoretical, simulation, and experimental results.

The design project will weighted as three lab reports and will graded somewhat more critically than the previous reports. Although the design project grade will in part depend on the write-up, the major criterion will be whether or not the circuit meets the design criteria.

7.6 Due Date

Friday, December 3, 2010 A. D. @ 5 pm Eastern Standard Time in the offices of Drs. Robinson or Brewer.